IEICE Electronics Express, Vol.16, No.18, 1–4

LETTER

A low-loss high-linearity SOI SP6T antenna switch using diode biasing method

Abdulraqeb Abdullah Saeed Abdo[1], **Jie Ling**[1a)], **and Pinghua Chen**[1]

Abstract This letter describes a single-pole six-throw (SP6T) antenna switch in a 180 nm silicon-on-insulator (SOI) CMOS technology for receive diversity and LTE transmit/receive applications. Using a new diode biasing method, the conventional biasing resistor and supply voltage are removed at the body of the stacked-FET switch, a diode is used to connect the body and gate for body bias instead. The biasing diode turns off and on and functions as a high and small resistor for the on and off state. The proposed design helps to achieve low loss and high linearity. The measured insertion loss (IL) at 0.9 and 1.9 GHz are roughly 0.29 and 0.46 dB, respectively. The switch shows a second harmonic of −86 and −83 dBc, and third harmonic power of −94 and −87 dBc with a +26 dBm input power at 0.9 and 1.9 GHz, respectively.

Keywords: silicon-on-insulator (SOI) switch, diode biasing, low loss
Classification: Integrated circuits

1. Introduction

As more and more communication standards such as Wideband Code Division-Multiple-Access (WCDMA), High-Speed Packet Access (HSPA), and 3GPP Long Term Evolution (LTE) are added into smart devices, multimode multiband front-end architectures are utilized. Besides, more wireless communication technologies such as 5G and Narrow Band Internet of Things (NB-IOT) are being integrated into mobile terminals [1]. Both trends lead to a greater need for RF switch components on front-end design of these devices [2, 3, 4].

Compared to the positive-intrinsic-negative (PIN) diode [5, 6], micro-electro-mechanical systems (MEMS) [7, 8], and gallium arsenide (GaAs) psuedomorphic high electron mobility transistor (pHEMT) [9, 10], Silicon-on-insulator (SOI) CMOS process shares the important features of being fast, reliable, and highly integratable, and thus, becomes a preferred choice for switch applications [11, 12, 13, 14]. The low break-down voltage and conductive substrate limit the standard bulk CMOS for RF switch applications [15, 16, 17]. In a partially-deleted (PD) technology [18], both floating body (FB) and body contacted (BC) FETs are offered [19]. The FB switches are beneficial to lower insertion loss (IL) whereas the BC switches achieve lower harmonics [20, 21]. To the contrary, the BC FET benefits the switch linearity due to the ability to prevent the junction diodes from forward biasing using negative body voltage bias [22, 23, 24], but the drawback with it is the increased loss [25, 26, 27].

This letter implements a single-pole six-throw (SP6T) antenna switch implemented in a 180 nm SOI CMOS process. To reduce the IL while maintaining excellent linearity, a stacked-FETs switch strategy employing BC devices with a novel diode biasing scheme has been proposed.

2. Circuit design

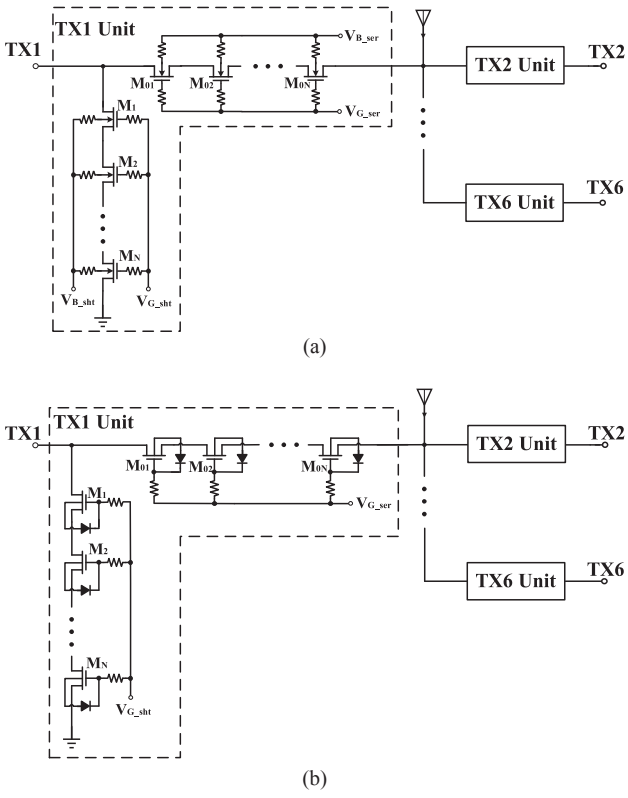


Fig. 1. SP6T switch with (a) traditional biasing method; (b) proposed diode biasing method.

As the ability to provide an advantage to reduce waveform distortion and improve linearity by applying a negative DC bias to the body to prevent the forward-bias of the junction diodes, the BC FET is employed as the switching device. Fig. 1(a) shows the traditional SP6T switch structure with BC-FET stacking strategy to improve the power handling capability [28]. Both the gate and body of the BC FETs

[1]Faculty of Computer, Guangdong University of Technology, Panyu Dist., Guangzhou 510006, P.R. China
a) jling@gdut.edu.cn

DOI: 10.1587/elex.16.20190494
Received August 1, 2019
Accepted August 8, 2019
Publicized August 30, 2019
Copyedited September 25, 2019

require a high resister to offer RF isolation for the biasing circuit and a biasing voltage to control the FET ON and OFF state for the switching. When the switch is in the ON state, bias voltage of +2.5 V and 0 V are applied, respectively, to the gate and body of the BC switch-FETs, whereas a −2.5 V bias voltage is applied to both gate and body in the OFF state. However, the major problem of the traditional switch structure is the additional wiring and contacts on and outside the BC stacked-FETs, as well as the need of biasing resistors and control voltage for the body. This results in more complex control and parasitic effect, and slightly larger chip size.

In allusion to the issues mentioned above, we propose a novel diode bias method for the BC SP6T switch, as shown in Fig. 1(b). The diode anode is connected to the body of the BC switch-FET whereas the cathode is tied to the gate. When a +2.5 V biasing voltage is applied to the switch-FET, the biasing diode would turn off which leads to a +2.5 V DC bias voltage at the gate and a slight positive voltage (near to zero) at the body, and thus, turning on the switch device. Also, when a −2.5 V biasing voltage is applied, the diode would be forward-biased and enables the body voltage of the BC switch-FET to maintain at nearly same negative DC potential as the gate.

Fig. 2 exhibits the SP6T equivalent circuit model when TX1 enabled. In contrast to the conventional version, the proposed scheme reduces the leakage loss for the body, leading to smaller on-state resistance. Since off-state capacitance is small enough, the IL from TX1 to antenna port can be simply expressed as:

$$\mathrm{IL} = 20log\left[1 + \frac{R_{on\_series}}{2Z_o}\right] \quad (1)$$

It is observed that from (1) that the new bias method is capable of achieving lower IL as it contributes to the decrease of the total on-state resistance R_{on_series}.

Fig. 3 depicts the simulated IL and second/third harmonics when the input power is +26 dBm of the two biasing method. It can be seen, on one hand, that the traditional and proposed switch biasing methods show similar low harmonics performance since both methods achieve almost same DC biasing voltage at the gate and body; on the other hand, the result agrees well with the analysis that the novel diode biasing method helps to reduce the IL of the proposed switch due to the absence of the biasing resistor and voltage supply for the body, which contributes to lower parasitic capacitance and loss.

Furthermore, the new bias scheme can achieve smaller chip area. Fig. 4 illustrates the top architecture of the designed SP6T antenna switch. The regulator and charge pump are utilized to generate adequate positive and negative biasing voltage, and a 3-bit GPIO CMOS/TTL-compatible control decoder is applied for path switching, and it is followed by a series of level shifters to shift the biasing voltage. It can be observed that the proposed bias strategy help to decrease the number of level shifters, control wiring and contacts on and outside the switch-FETs by removing the body resistor and voltage supply, and thus, reducing chip size and cost.

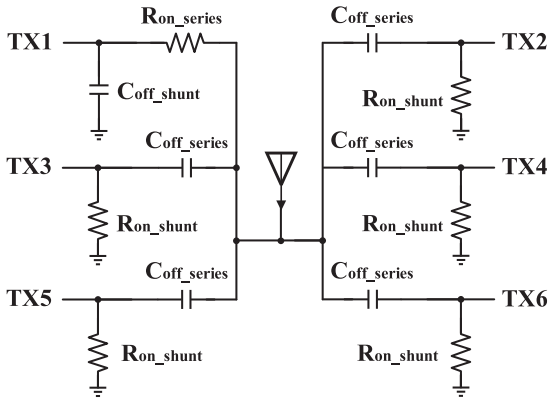


Fig. 2. SP6T equivalent circuit model when TX1 enabled

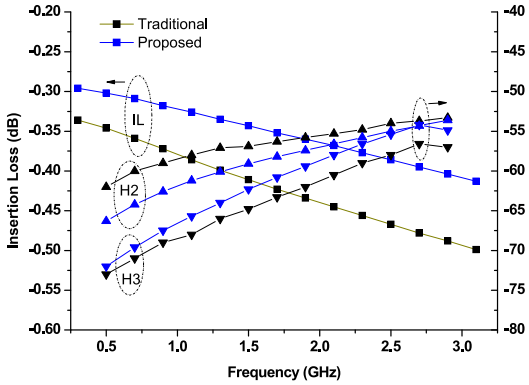


Fig. 3. Simulated IL and harmonics when the input power is +26 dBm of the two biasing methods. Switching-FET width of 3000 μm and length of 0.32 μm are used in simulation.

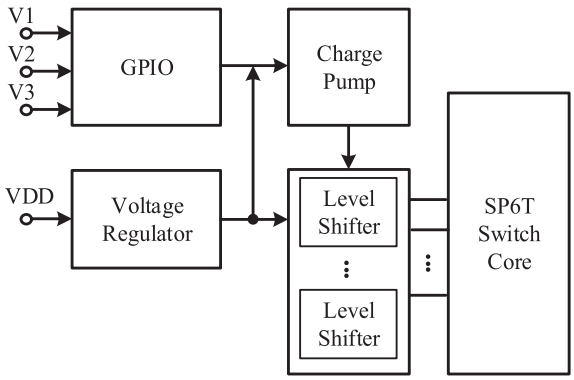


Fig. 4. SOI SP6T antenna switch top architecture.

3. Fabrication and results

Fig. 5 shows the chip photo of the proposed SP6T antenna switch using diode biasing method with a size of 1000 × 750 μm^2. Each TX unit consists of a series chain and a shunt chain. Both series and shunt chains have 8 stacked-FETs switch devices. The device width of the series and shunt stacked-FETs devices are set as 3000 and 500 μm, respectively, which is optimized for the trade-off of the IL, isolation, and linearity performance.

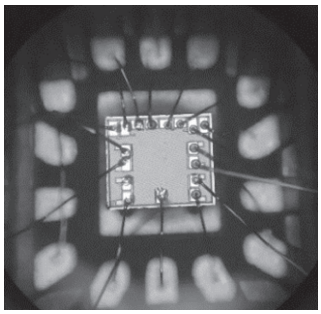
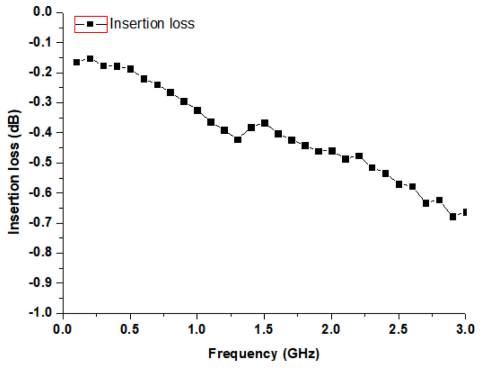
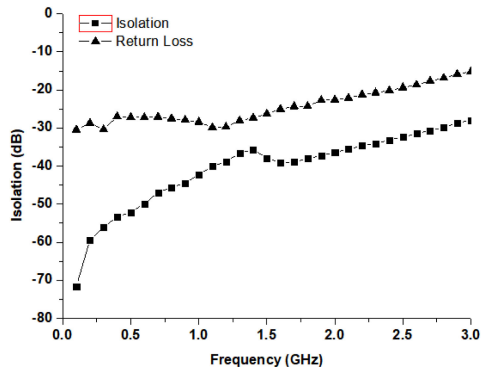


Fig. 5. Chip photo of proposed SOI SP6T antenna switch.



(a)

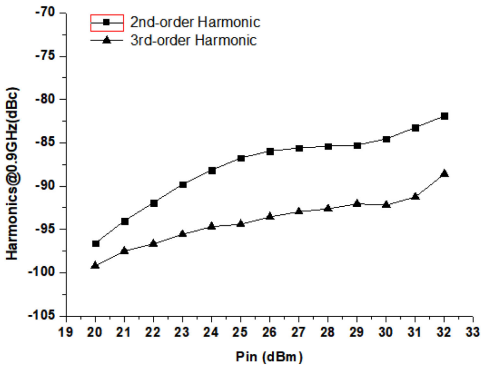


(b)

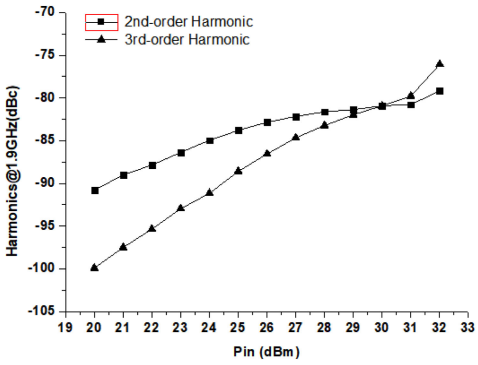
Fig. 6. De-embedded measurement results of proposed SP6T switch: (a) IL; (b) Isolation and Return Loss.

Fig. 6(a) and (b) plot the de-embedded measurement IL, isolation and return loss of the proposed SOI SP6T antenna switch from 0 to 3.0 GHz. The SP6T switch exhibits low IL of 0.29 dB at 0.9 GHz and 0.46 dB at 1.9 GHz. These results agree well with the analysis that the proposed switch can achieve lower IL with the use of the new diode biasing strategy. The isolation is roughly 44 dB at 0.9 GHz and 37.2 dB at 1.9 GHz, while the RL is around 27.9 dB and 22.7 dB at 0.9 and 1.9 GHz, respectively.

The 2nd- and 3rd-order harmonic responses at 0.9 and 1.9 GHz are measured and depicted in Fig. 7(a) and (b), respectively. With a +26 dBm input power, the 2nd- and 3rd-order harmonic are −86 dBc and −94 dBc at 0.9 GHz, and −83 dBc and −87 dBc at 1.9 GHz. It can be seen that the SP6T switch reveals low 2nd- and 3rd-order harmonics,



(a)



(b)

Fig. 7. Measurement results of the 2nd- and 3rd-order harmonic powers for the proposed SP6T switch at the fundamental frequencies of: (a) 0.9 GHz; (b) 1.9 GHz.

which demonstrates that the proposed diode biasing method, without using extra biasing resistor and DC supply for the body, is able to achieve low harmonic distortion and high linearity.

Table I compares the switch performance of this letter and other published works. In contrast to other SOI-CMOS switches, the proposed SP6T switch achieves competitive IL, isolation, RL, and harmonic distortion. The switch obtains a low IL of 0.29 and 0.46 dB at 0.9 and 1.9 GHz, respectively, which is lower than those of other reported works. It can be concluded that the proposed switch using the novel diode biasing method provides an advantage to reduce the IL, and meanwhile, maintains favorable harmonic and linearity performance.

Table I. Performance comparison of the two switches.

	This letter		[29]		[30]		[31]	
SPXT	SP6T		SP4T		SP6T		SP16T	
f (GHz)	0.9	1.9	0.9	1.9	0.9	1.9	0.9	1.9
IL (dB)	0.29	0.46	0.5	0.6	0.51	0.69	1	1.1
ISO (dB)	44	37	31	23	49	38	38	35
RL (dB)	28	23	20–25		22	16	22	26
H2 (dBc)*	−86	−83	−75	−81	−86	−83	−91	−94
H3 (dBc)*	−94	−87	−81	−78	−104	−95	−86	−86

*Input power P_{IN} = +26 dBm

4. Conclusion

A low-loss and high-linearity SP6T antenna switch using a diode to connect the body and gate of the BC switch-FET without employing the biasing resistor and supply voltage to the body, has been implemented in a 180 nm SOI CMOS process. The new body bias strategy achieves an analogous DC bias as the traditional structure, which helps to reduce the IL without degrading the linearity performance. The switch shows the IL of 0.29 and 0.46 dB, second-order harmonics of −86 and −83 dBc, and third-order harmonics of −94 and −87 dBc with a +26 dBm input power at 0.9 and 1.9 GHz, respectively. In conclusion, the diode biasing method is a suitable way to achieve high-performance switches.

References

[1] G. A. Akpakwu, *et al.*: "A survey on 5G networks for the internet of things: Communication technologies and challenges," IEEE Access **6** (2017) 3619 (DOI: 10.1109/ACCESS.2017.2779844).

[2] Z. H. Zhang, *et al.*: "Dual SPDT/SP3T SOI CMOS switch adopting alternative bias strategy with enhanced performance compared to the conventional case," IEICE Electron. Express **13** (2016) 20160322 (DOI: 10.1587/elex.13.20160322).

[3] Q. Chaudhry, *et al.*: "A linear CMOS SOI SP14T antenna switch for cellular applications," IEEE Radio Frequency Integr. Circuits Symp. (2012) 155 (DOI: 10.1109/RFIC.2012.6242253).

[4] B. K. Esfeh, *et al.*: "A SPDT RF switch small- and large-signal characteristics on TR-HR SOI substrates," IEEE SOI-3D-Sub-threshold Micro-electron. Tech. Unified Conf. (S3S) (2017) 1 (DOI: 10.1109/S3S.2017.8308737).

[5] Y. B. Chaouche, *et al.*: "Design of reconfigurable fractal antenna using pin diode switch for wireless applications," IEEE Mediterranean Microw. Symp. (2016) 1 (DOI: 10.1109/MMS.2016.7803852).

[6] D. R. Jahagirdar, *et al.*: "Design and development of high power SP9T switch," IEEE Int. Conf. on Antenna Inno. & Modern Tech. for Ground, Aircraft and Satellite Applications (iAIM) (2017) 1 (DOI: 10.1109/IAIM.2017.8402552).

[7] R. George, *et al.*: "Design of series RF MEMS switches suitable for reconfigurable antenna applications," Int. Conf. on Circuit, Power and Computing Tech. (2017) 1 (DOI: 10.1109/ICCPCT.2017.8074405).

[8] Y. H. Liu, *et al.*: "High-power high-isolation RF-MEMS switches with enhanced hot-switching reliability using a shunt protection technique," IEEE Trans. Microw. Theory Techn. **65** (2017) 3188 (DOI: 10.1109/TMTT.2017.2687427).

[9] C.-J. Wei, *et al.*: "Multi-gate pHEMT modeling for switch applications," 2012 IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS) (2012) 1 (DOI: 10.1109/CSICS.2012.6340063).

[10] N. Lu and R. J. Weber: "The design of high linearity pHEMT switches," IEEE Int. Midwest Symp. on Circuits and Syst. (2010) 1 (DOI: 10.1109/MWSCAS.2010.5548786).

[11] F. Gianesello, *et al.*: "Highly linear and sub 120 fs Ron × Coff 130 nm RF SOI technology targeting 5G carrier aggregation RF switches and FEM SOC," IEEE 16th Topical Meeting on Silicon Monolith. Integr. Circuits in RF Syst. (SiRF) (2016) 9 (DOI: 10.1109/SIRF.2016.7445454).

[12] M. Jaffe, *et al.*: "Improvements in SOI technology for RF switches," IEEE 15th Topical Meeting on Silicon Monolith. Integr. Circuits in RF Systems (2015) 30 (DOI: 10.1109/SIRF.2015.7119865).

[13] A. Joseph, *et al.*: "Power handling capability of an SOI RF switch," IEEE Radio Frequency Integr. Circuits Symp. (2013) 3 (DOI: 10.1109/RFIC.2013.6569611).

[14] B. Yu, *et al.*: "Ultra-wideband low-loss switch design in high-resistivity trap-rich SOI with enhanced channel mobility," IEEE Trans. Microw. Theory Techn. **65** (2017) 3937 (DOI: 10.1109/TMTT.2017.2696944).

[15] S. Wang and Z.-K. Li: "A 6–32 GHz T/R switch in 0.18-μm CMOS technology," IEICE Electron. Express **9** (2012) 590 (DOI: 10.1587/elex.9.590).

[16] M. Ahn, *et al.*: "A high-power CMOS switch using a novel adaptive voltage swing distribution method in multistack FETs," IEEE Trans. Microw. Theory Techn. **56** (2008) 849 (DOI: 10.1109/TMTT.2008.919047).

[17] J. Rascher, *et al.*: "Highly linear robust RF switch with low insertion loss and high power handling capability in a 65 nm CMOS technology," IEEE 12th Topical Meeting on Silicon Monolith. Integr. Circuits in RF Syst. (2012) 1 (DOI: 10.1109/SiRF.2012.6160157).

[18] H. Lee, *et al.*: "Analysis of body bias effect with PD-SOI for analog and RF applications," Solid-State Electron. **46** (2002) 1169 (DOI: 10.1016/S0038-1101(02)00011-4).

[19] M. Ahn, *et al.*: "Ultra low loss and high linearity SPMT antenna switch using SOI CMOS process," IEEE European Microw. Conf. (2010) 652 (DOI: 10.23919/EUMC.2010.5616264).

[20] Z. H. Zhang, *et al.*: "Effects and contrasts of silicon-on-insulator floating-body and body-contacted field-effect transistors to the design of high-performance antenna switches," IET Microw., Antennas & Propagat. **10** (2016) 507 (DOI: 10.1049/iet-map.2015.0487).

[21] D. Wang, *et al.*: "High performance SOI RF switches for wireless applications," Solid-State and Integr. Circuit Techn. Conf. (2010) 611 (DOI: 10.1109/ICSICT.2010.5667307).

[22] A. Tombak, *et al.*: "Design of high-order switches for multimode applications on a silicon-on-insulator technology," IEEE Trans. Microw. Theory Techn. **61** (2013) 3639 (DOI: 10.1109/TMTT.2013.2277989).

[23] X. S. Wang and C. P. Yue: "A dual-band SP6T T/R switch in SOI CMOS with 37-dBm P-0.1 dB for GSM/W-CDMA handsets," IEEE Trans. Microw. Theory Techn. **62** (2014) 861 (DOI: 10.1109/TMTT.2014.2308306).

[24] J. Cui, *et al.*: "A linear 180 nm SOI CMOS antenna switch module using integrated passive device," J. Semicond. **35** (2014) 065005 (DOI: 10.1088/1674-4926/35/6/065005).

[25] D. Im, *et al.*: "A stacked-FET linear SOI CMOS cellular antenna switch with an extremely low-power biasing strategy," IEEE Trans. Microw. Theory Techn. **63** (2015) 1964 (DOI: 10.1109/TMTT.2015.2427801).

[26] D. Im and K. Lee: "Characterization and optimization of partially depleted SOI MOSFETs for high power RF switch applications," Solid-State Electron. **90** (2013) 94 (DOI: 10.1016/j.sse.2013.02.046).

[27] H. Zhu, *et al.*: "Ultra low loss and high linearity RF switch using 130 nm SOI CMOS process," IEEE 12th Int. Conf. on ASIC (ASICON) (2017) 698 (DOI: 10.1109/ASICON.2017.8252571).

[28] D. Im and K. Lee: "Stacked-FET linear SOI CMOS SPDT antenna switch with input P1dB greater than 40 dBm," IEICE Electron. Express **9** (2012) 1813 (DOI: 10.1587/elex.9.1813).

[29] Skyworks, Product datasheet, SKY13388-465LF[Online]. Available: http://www.skyworksinc.com/uploads/documents/SKY13388_465LF_201403H.pdf.

[30] V. Blaschke, *et al.*: "A linear-throw SP6T antenna switch in 180 nm CMOS thick-film SOI," IEEE Microw., Commun., Antennas and Electron. Syst. Conf. (2011) 1 (DOI: 10.1109/COMCAS.2011.6105898).

[31] J. Cui, *et al.*: "Monolithic single-pole sixteen-throw T/R switch for next-generation front-end module," IEEE Microw. Wireless Compon. Lett. **24** (2014) 345 (DOI: 10.1109/LMWC.2014.2309082).