LETTER

A wideband current-reuse-RGC TIA circuit with low-power consumption

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Abstract This paper presents a new Gain-Adder (GA) circuit for Current-Reuse (CR)-RGC TIA. The proposed GA circuit employs one transistor alone to enhance bandwidth and decrease power consumption. The proposed CR-RGC TIA circuit is designed in a 65-nm CMOS technology. The simulation results confirmed that the proposed CR-RGC TIA circuit improves bandwidth by 83% and decreases the power consumption by 34% in comparison with the conventional one.
Keywords: transimpedance amplifier, current-reuse, regulated-cascode
Classification: Integrated circuits

1. Introduction

The increase of network traffic requires more high-speed and large-capacity communications for optical networks [1, 2]. Accordingly, data traffic in a data center is explosively growing [3, 4], and the power consumption is also increasing due to a large number of pieces of communication equipment [5, 6, 7]. In the optical communication systems, a transimpedance amplifier (TIA) [8], which converts currents of a photodiode to voltage signals and amplifies it to drive following circuits, is the most essential circuit for the frequency bandwidth of the optical receiver [9, 10, 11], but to achieve high-performance transimpedance, TIAs require large power consumption [12]. A low power TIA is also being actively investigated [13, 14].

This paper proposed a new circuit topology for bandwidth enhancement with low-power consumption based on a current-reuse regulated-cascode (CR-RGC) TIA. The conventional CR-RGC TIA [15, 16, 17, 18] has the gain-adder (GA) circuit consisting of two inverters and a load resistor for the first stage amplifier. The proposed GA circuit is simplified with a transistor alone to reduce the power consumption without bandwidth degradation. We designed the proposed TIA in a 65-nm CMOS technology. The simulation results confirmed that the proposed circuit increases the bandwidth by 83% and decreases the power consumption by 34% in comparison with the conventional CR-RGC TIA.

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2. Conventional CR-RGC TIA circuit

In the receivers of high-speed optical communication systems, a photodiode connects with the input port of the TIA [19], and the TIA converts the photocurrent signals to the voltage signals. Its frequency bandwidth is determined by the dominant pole generated by capacitors and resistances including photodiode junction and input impedance of TIAs [20]. Therefore, the bandwidth can be improved by lower the input impedance of TIAs [21]. Consequently, a regulated-cascode (RGC) circuit [22, 23, 24, 25] is widely used for a wideband TIA because it has a low-input impedance characteristic, and various modified RGC circuits are investigated [26, 27].

For more reducing the input impedance, a CR-RGC TIA using a current-reuse (CR) technique [28] based on the RGC TIA has been proposed [16]. Fig. 1 shows the circuit diagram of the conventional CR-RGC TIA. It is configured with series connected NMOS and PMOS common gate circuits and the regulated feedback path to the gate port of them. This configuration boosts the transconductance of first stage to $g_{mN} + g_{mP}$ ($\approx 2g_m$), which is about twice in the conventional RGC TIA. Accordingly, the input impedance Z'_{in} of the CR-RGC TIA circuit is written as follows:

$$Z'_{in} = \frac{1}{(g_{mN} + g_{mP})(1 + A)} \approx \frac{1}{2g_m(1 + A)} \quad (1)$$

where A is the amplification of the feedback path in the RGC circuit.

On the other hand, the transimpedance gain $Z_t(s)$ is written as,

$$Z_t(s) = \frac{Z_{t0}}{(1 + s/s_1)(1 + s/s_2)}, \quad (2)$$

where s_1 and s_2 are the first and second poles of the CR-RGC TIA, respectively [29]. The low-frequency transimpedance gain Z_{t0} is expressed as Eq. (3).

$$Z_{t0} = g_{mi}R_D R, \quad R := R_N = R_P, \quad (3)$$

where g_{mi} is a transconductance of inverters, and R_D is a load resistor. The poles s_1 and s_2 are written as follows:

$$s_1 = \frac{1}{R_1 C_1} = \frac{1}{Z'_{in} C_{in}}, \quad (4)$$

$$s_2 = \frac{1}{R_2 C_2} = \frac{1}{R\{C_N + C_{inv}(1 + g_{mi}R_D)\}}, \quad (5)$$

Fig. 1. Circuit diagram of conventional CR-RGC TIA.

$$C_2 = C_N + C_{inv}(1 + g_{mi}R_D)$$
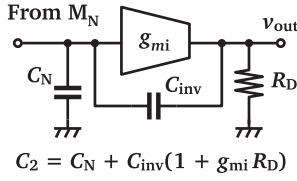
Fig. 2. Parasitic capacitors defining second pole of conventional RC-RGC TIA.

where C_{in} ($= C_{PD} + C_{TIA}$) is an input capacitance, C_{inv} ($= C_{gd;iN} + C_{gd;iP}$) is a gate-drain capacitance in the GA circuit, and C_N is a parasitic capacitance at the drain of the NMOS M_N. In Eq. (5), $C_{inv}(1 + g_{mi}R_D)$ is the Miller capacitance [30] as shown in Fig. 2. In the conventional circuit, the GA circuit uses two inverters which have the large gain $g_{mi}R_D$, and it makes s_2 to close to s_1. That means the frequency bandwidth depends on not only s_1 but also s_2. Furthermore, the GA circuit requires bias circuits for the two inverters, and a through current flows by them, it causes to increase power consumption.

3. Proposed CR-RGC TIA

To overcome these problems, we propose a new CR-RGC TIA topology that can extend the frequency bandwidth with low-power consumption, as shown in Fig. 3. It employs the simple GA circuit consists of one transistor M_f alone instead of two inverters.

Fig. 4 shows the operational principle of the proposed GA circuit. The current i_{Mf} that is a part of the signal current i_{MP} flows to R_N, and it joins i_{MN} generated by M_N. As a result, the output voltage v_N is generated by a total current of two RGC circuits. This GA circuit topology can reduce power consumption because it can prevent through current since no inverters.

Let us consider a frequency characteristic of the proposed topology. The first pole s_1 is equal to the conventional TIA as written Eq. (5). The capacitance C_2 making second pole s_2 is given by $C_N + C_{gs}$ as shown in Fig. 5. It is confirmed that the Miller effect of the C_{gs} is smaller than the conventional one because the gain of the source follower is small. The second pole of the proposed circuit is expressed as

$$s_2 = \frac{1}{R_2 C_2} = \frac{1}{R(C_N + C_{gs})} . \tag{6}$$

Consequently, the second pole of the proposed TIA is higher than the conventional one from Eq. (5) and (6). As a result, the frequency bandwidth of the proposed TIA can be expanded.
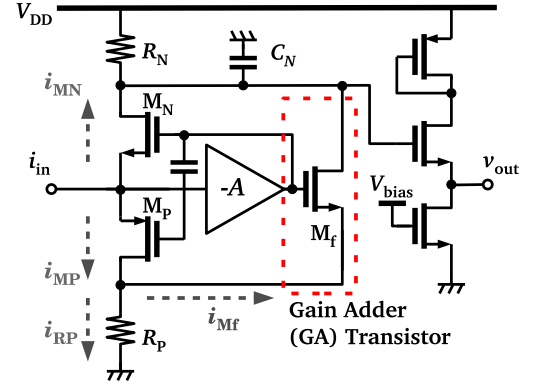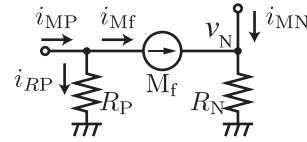

Fig. 3. Circuit diagram of proposed CR-RGC TIA.

Fig. 4. Operational principle of GA circuit.
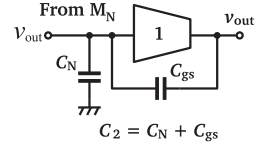

$$C_2 = C_N + C_{gs}$$

Fig. 5. Parasitic capacitors defining second pole of proposed CR-RGC TIA.

The low-frequency transimpedance gain $Z_t(0)$ of the proposed CR-RGC TIA is given as Eq. (7)

$$Z'_{t0} = \frac{1}{2}\left(1 + \frac{g_{mf}}{g_m}\right)R, \quad R := R_N = R_P, \tag{7}$$

here, g_m is the transconductance of M_N and M_P, g_{mf} is transconductance of M_f, and the gain of the source follower is assumed to be 1. It is confirmed that the gain of proposed topology decreases compared with Eq. (3). However, its influence is smaller than the expansion of frequency bandwidth, and the proposed topology has advantage regarding a gain-bandwidth (GB) product. The proposed circuit has an asymmetrical GA circuit using the transistor M_f. However, the delay time of the M_f is very small and thus will almost not worsen waveforms.

4. Simulation results

The proposed CR-RGC TIA is designed in a 65-nm CMOS technology with the 1.8 V supply. Fig. 6 shows the circuit configuration of the proposed CR-RGC TIA. Common-source amplifiers are employed as the local-feedback and output buffer. The buffer is connected from the output of the source follower and boosts the transimpedance gain to arrange the total gain of the proposed TIA in the previous one for the comparison of specifications.

The simulated results of frequency responses for the conventional and proposed TIAs are shown in Fig. 7. The frequency bandwidth f_{-3dB} and the transimpedance gain
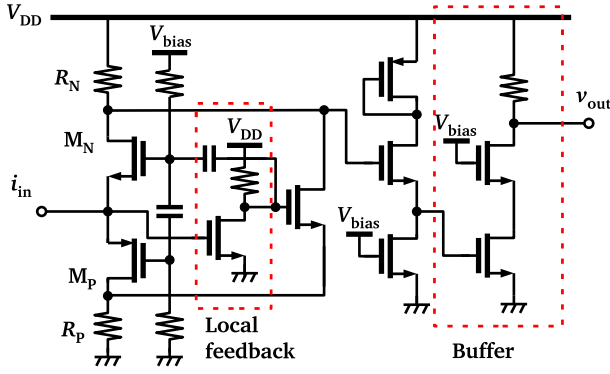
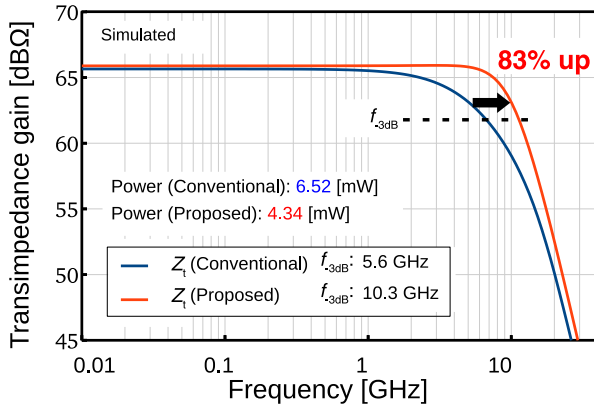**Fig. 6.** Simulation circuit of proposed CR-RGC TIA.

**Fig. 7.** Frequency responses of transimpedance gain.

Z_{t0} of our circuit are 10.3 GHz and 65.8 dBΩ, respectively. In comparison with the conventional TIA, the bandwidth of the proposed TIA improves by 83% with the same Z_{t0} condition.

Fig. 8 shows the GB products and power consumptions for various load resistances $R_{N,P}$. When the load resistances R ($= R_N = R_P$) increase, the GB products of both circuits become large. The GB products of the conventional circuit are saturated over the load resistance 500 Ω. In the proposed circuit, in contrast to the previous one, it grows over 500 Ω because the second pole locates at more higher-frequency than the conventional circuit. If we use large load resistances, the electrical currents of $M_{N,P}$ become small, therefore the bias currents of the GA circuits
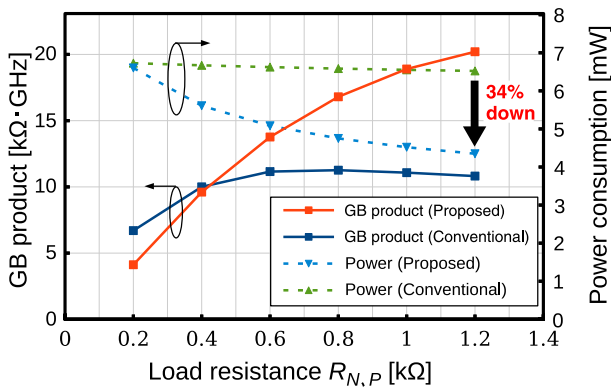

Fig. 8. GB product and power consumption characteristics for various load resistances $R_{N,P}$.

play a dominant role in TIAs. As mentioned earlier, the bias current of the proposed GA circuit is smaller than the conventional one. As a result, the power consumption of the proposed circuit becomes small.

Fig. 9 shows the eye diagrams with 10 Gbit/s data rate in the conventional and proposed CR-RGC TIA circuits, where T_r and T_f are a rise and fall time from 10% to 90% of the amplitude. Note that, the amplitudes of them are almost the same; however the offset voltage of the proposed circuit is higher than the conventional one because they have different output stages. These results confirm that T_r and T_f are about 29 picoseconds shorter, and that the eye-opening is clear than the conventional TIA. These results reflect the bandwidth enhancement of the proposed circuit.
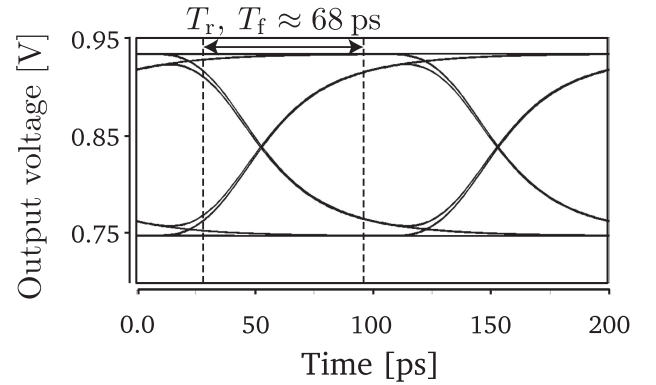
(a) Conventional CR-RGC TIA
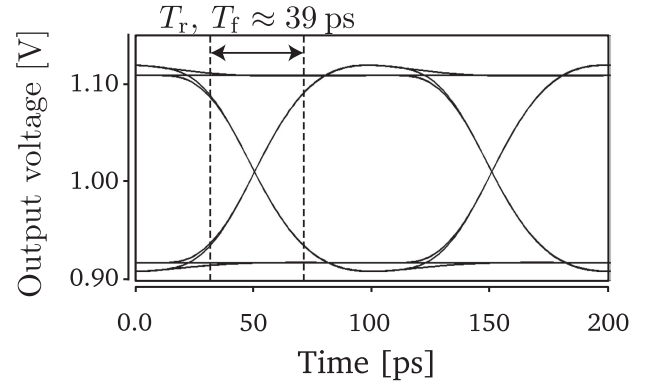
(b) Proposed CR-RGC

Fig. 9. Eye diagrams of conventional and proposed TIA (bit rate: 10 Gbit/s).

Table I summarizes the performance of the proposed and conventional circuits. The figure-of-merit (FOM) is defined as the GB product per power consumption. This table confirms that the FOM value of the proposed circuit was larger than the conventional one. It means wide-bandwidth and low-power consumption.

In optical communication systems, a photodiode which has a large stray capacitance is connected to the input port of the TIA, hence the dominant pole locates at the input port. The influence of the pole associated with a layout is smaller than the dominant pole, therefore we seem that the proposed circuit can achieve the good performance to the conventional one even on a circuit experiment.

Table I. Performance summary and comparison.

	Proposal	Conventional
Power (mW)	4.34	6.52
Gain (dBΩ)	65.8	65.6
f_{3dB} (GHz)	10.3	5.6
FOM (Ω·GHz/mW)	4,628	1,636

*simulated results

5. Conclusion

We proposed a new circuit topology for bandwidth enhancement with low-power consumption based on a CR-RGC TIA. The simple GA circuit that has one transistor alone instead of two inverters enables to lower the power consumption without degradation of bandwidth. The proposed CR-RGC TIA was designed with a 65-nm CMOS technology and simulated. The simulated results confirmed that the proposed circuit technique enables to improve bandwidth by 83% and to decrease the power consumption by 34% in comparison with the conventional one. It will contribute to low-power consumption and high-speed optical interconnection systems.

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