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LETTER

A wideband low-jitter PLL with an optimized Ring-VCO

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Abstract A wideband low-jitter phase-locked loop (PLL) is proposed to provide high performance clocks for the transceivers. The ring voltage-controlled oscillator (Ring-VCO) is a key component of a PLL, which directly determine the out-band phase noise and output frequency range of the PLL. Therefore, a low phase noise two-stage Ring-VCO with a novel delay cell is proposed to help achieve a wideband low-jitter PLL. An accumulation-mode MOS (AMOS) varactor pair is adopted in the delay cell to improve the fine tuning linearity. Moreover, an additional AMOS varactor pair is employed to reduce the VCO gain variation in the coarse tuning process and enhance the tolerance in temperature and voltage variations. Implemented in a conventional TSMC 180 nm CMOS process, the proposed Ring-VCO can tune from 0.73 to 1.92 GHz and the worst-case phase noise at 1 MHz offset is −102 dBc/Hz. The output frequency range of the proposed PLL is 0.06–1.92 GHz and the RMS jitter is less than 3.8 ps over the whole working band.

Keywords: phase-locked loop (PLL), ring voltage-controlled oscillator (Ring-VCO), VCO gain variation, phase noise, jitter
Classification: Integrated circuits

1. Introduction

Phase-Locked Loops (PLLs) are widely employed to generate high quality clocks for many applications such as mixers, analog-to-digital converters (ADCs), and I/O interfaces [1, 2, 3, 4, 5]. Jitter is a key characteristic to define the uncertainty of the sampling moments in ADCs and determine the bit error-rate in the system. A PLL which multiplies low frequency reference clocks to generate high frequency clocks is usually designed with a ring voltage-controlled oscillator (Ring-VCO) or an LC-tank VCO (LC-VCO). An LC-VCO shows high sensitivity to magnetic coupling and occupies large silicon area. Hence, the Ring-VCO based PLL is preferable in applications due to its small area, wide range of tuning property, high insensitivity to magnetic coupling, and easy integration. The poor jitter performance of the Ring-VCO based PLL, however, brings difficulties in providing high quality clocks [6, 7, 8, 9].

Several methods have been used to reduce the jitter of a Ring-VCO based PLL. The sub-sampling PLLs (SSPLLs) [10, 11, 12] are representative designs to realize excellent jitter performance, which suffer from the limited frequency acquisition range. In [13, 14, 15, 16, 17], injection-locked PLLs are employed to reduce the jitter, however, additional calibration circuits are usually required to guarantee the optimal performance and the correct operation. An attractive method uses hybrid loops to achieve low jitter PLLs [18, 19, 20], as well as results in rather complicated circuits. More and more digital PLLs [21, 22, 23, 24, 25, 26] are designed due to the advantages in terms of power, area, and programmability, whereas the improvement is needed in the jitter performance of digital PLLs. The Ring-VCO is the most important component of the PLL, in which the low phase noise and wideband characteristics directly determine the jitter and frequency range of PLLs. This paper proposes a low phase noise two-stage Ring-VCO with a novel delay cell to help achieve a wideband low-jitter PLL. An accumulation-mode MOS (AMOS) varactor pair is adopted in the delay cell to improve the fine tuning linearity. Moreover, an additional AMOS varactor pair is employed to reduce the VCO gain (K_{vco}) variation in the coarse tuning process and enhance the tolerance in temperature and supply voltage variations. The measured result shows that the proposed Ring-VCO realizes wideband output, small K_{vco} variation, and low phase noise. The proposed PLL achieves 0.06–1.92 GHz output frequency range together with low jitter.

The rest of this paper is organized as follows. In section 2, the design of the proposed Ring-VCO is described. Section 3 introduces the proposed wideband low-jitter PLL. In section 4, the measurement results of the Ring-VCO and PLL chips are presented. Finally in section 5, conclusions are drawn.

2. The proposed Ring-VCO

The top architecture of a Ring-VCO with two-stage delay cells is illustrated in Fig. 1(a). Since each delay cell contributes noise, the two-stage structure can achieve lower phase noise compared with three or more stages designs [27]. The delay cell utilized in [28] is sketched in Fig. 1(b), which is made up of transmission gates and small cross-coupled inverters. The delay time and oscillation condition are mainly determined by the inverters of X_1 and X_2 and the positive feedback inverter pair (X_3, X_4) forms a latch which speeds up the transition. The phase noise of the two-stage Ring-VCO is inversely proportional to the transition speed and consequently a low phase noise is achieved. A transmission gate whose resistance is adjusted by varying the gate voltage is used for the fine tuning, however, the structural property of the MOS transistor makes K_{vco} change a lot with the tuning voltage (vtune). Low threshold voltage MOS transistors are usually employed in the transmission gate to enlarge the tuning range, whereas the K_{vco}

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variation is still large. A significant variation in K_{vco} would have influences on switching speed, phase noise, and loop bandwidth of a PLL. To minimize the K_{vco} variation and phase noise, an optimized delay cell shown in Fig. 2 is proposed. In addition to the inverters of X_1–X_4, the delay cell also includes AMOS varactor pairs and a metal-insulator-metal (MIM) capacitor bank. To achieve wide frequency range together with low K_{vco}, the 4-bit switched MIM capacitor bank is utilized. In the locking process of the PLL, a coarse tuning is firstly accomplished by an automatic frequency control (AFC) to choose a specific sub-band, after which a fine tuning is proceeded. As illustrated in Fig. 2, an AMOS varactor pair is adopted for fine tuning instead of transmission gates, which can effectively improve the tuning linearity. Fig. 3 illustrates a comparison of tuning characteristic between the applications of transmission gates and AMOS varactors. The tuning linearity is obviously improved by using AMOS varactors, which is beneficial to the stability of the PLL, the integration of loop filter, and the optimization in PLL performances.

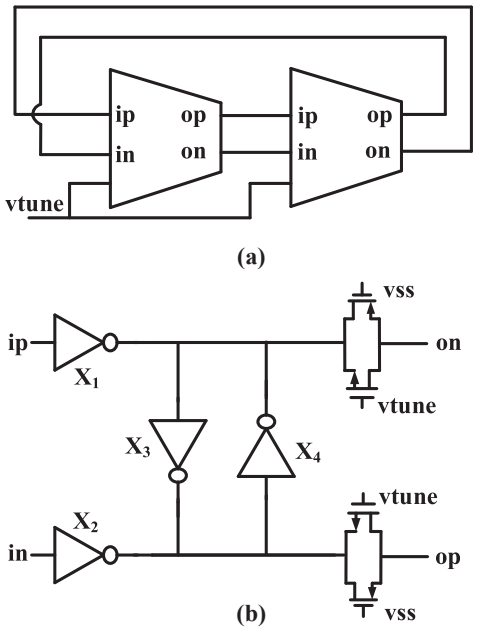

Fig. 1. Two-stage Ring-VCO (a) top-level, and (b) delay cell using transmission gates.

As shown in Fig. 4, the half-circuit of the delay cell is investigated for deriving the oscillation frequency of the proposed Ring-VCO. The g_{mp1} and g_{mn1} represent the transconductance of the MOS transistors in the input inverter, and the transconductance of the positive feedback inverter is described by g_{mp2} and g_{mn2}. The transfer function is expressed as

$$H(s) = \frac{V_o}{V_{in}} = \frac{g_{mn1} + g_{mp1}}{g_{mn2} + g_{mp2} - G_L - sC_L} \tag{1}$$

where C_L represents all the equivalent capacitances, $G_L = g_{dp1} + g_{dp2} + g_{dn1} + g_{dn2}$, the g_d is the channel conductance. The Ring-VCO must satisfy the Barkhausen criteria to maintain the oscillation. The operating frequency is

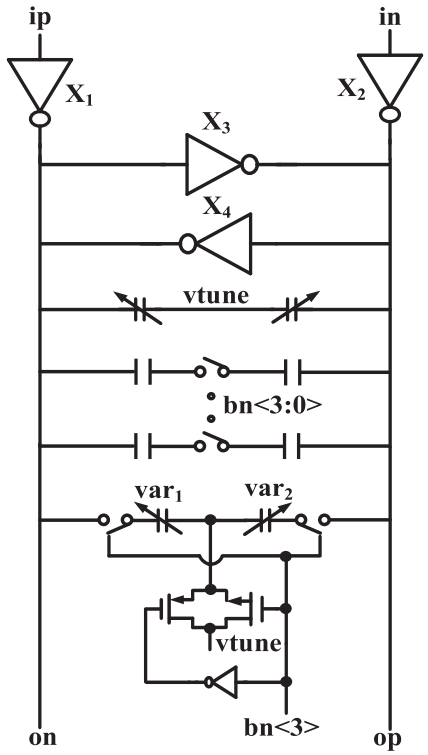

Fig. 2. The proposed delay cell.

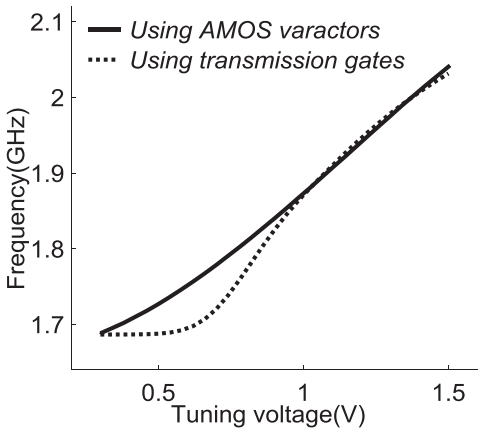

Fig. 3. The tuning characteristics when using transmission gates or AMOS varactors.

given as equation (2) by equating the voltage gain to unity.

$$\omega_0 = \frac{\sqrt{(g_{mn1} + g_{mp1})^2 - (G_L - g_{mn2} - g_{mp2})^2}}{C_L} \tag{2}$$

Referring to (2), the frequency is closely related to the transconductance which varies with the temperature and supply voltage. Each sub-band tuning curve must realize a large enough tuning range to withstand the changes in temperature and voltage. Hence, an additional AMOS varactor pair of var_1 and var_2 shown in Fig. 2 is employed to enlarge the tuning range in the lower half of the entire sub-bands, and thus enhancing the tolerance in temperature and supply voltage variations. The K_{vco} variation across different sub-bands is also reduced by using var_1 and var_2.

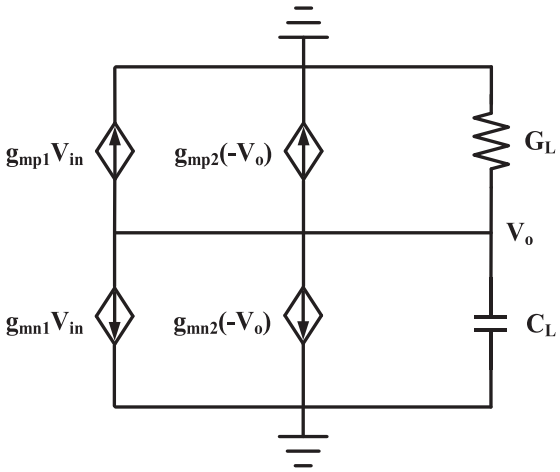

Fig. 4. Half circuit for frequency analysis.

3. The proposed wideband low-jitter PLL

The proposed wideband low-jitter PLL is given in Fig. 5, which is composed of a charge pump (CP), a 3-order loop filter (LF), a 3-order ΔΣ modulator (DSM), a phase switching multi-modulus divider (PS-MMD), a phase frequency detector (PFD), an AFC, a Ring-VCO, and an output divider (OD). The PFD compares the timing/phase between a feedback divider clock (F_{DIV}) and a reference clock (F_{REF}). The CP converts the PFD output signals which contain the information of timing/phase errors into currents for discharging or charging the LF, and the output of LF controls the Ring-VCO. The PS-MMD and DSM are used to realize fractional frequency division function, and the AFC is employed to help achieve coarse tuning in the PLL locking process. The OD is usually used between the Ring-VCO and PLL output to enlarge output frequency range.

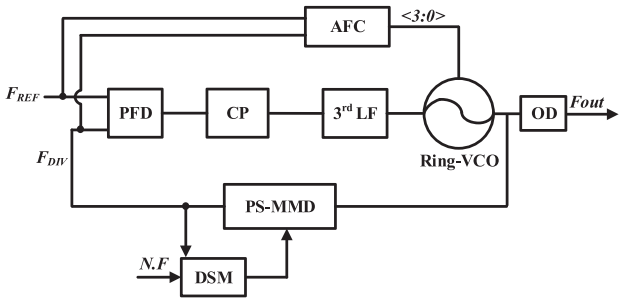

Fig. 5. The proposed PLL.

The PFD consists of CMOS logic gates and D-flip flops (DFFs). When the phase error between F_{REF} and F_{DIV} approaches zero, the PFD cannot output correct little pulse signal as a result of non-ideal factors, and then the dead region appears. A delay cell is often added in PFD to avoid dead-brand region, and the generated finite width pulse signal should guarantee that no dead-zone occurs and the noise contribution of the CP is minimized. The CP is optimized using two rail-to-rail operational amplifiers and the OD is designed using true-single-phase-clock (TSPC) DFFs. It is worth noting that a PS-MMD made up of a digital controller, a phase selector, and divide-by-2/3 cells is employed to suppress the quantization noise [29, 30, 31], which achieves a division ratio range of 4–63 with a division step of 0.25.

4. Results and discussions

The micrograph of the proposed PLL fabricated using a conventional TSMC 180 nm CMOS process is shown in Fig. 6 and the chip occupies 410 μm × 240 μm excluding the I/O pads. The PLL utilizes a F_{REF} of 48 MHz and an external loop filter is employed for greater flexibility and the best jitter performance. In order to verify the performances of the proposed Ring-VCO, a single chip of the Ring-VCO was designed and measured. The tuning characteristic and phase noise of the Ring-VCO are illustrated in Fig. 7. A frequency tuning range of 0.73–1.92 GHz is achieved as shown in Fig. 7(a) and the K_{vco} varies from 256 to 290 MHz/V with a variation of less than 6.2%. The small K_{vco} variation is beneficial to the phase noise, switching speed, and stability of the PLL. The simulated and measured phase noises at 1 MHz offset are shown in Fig. 7(b), which are less than −102 dBc/Hz. The measured results of the Ring-VCO show that the proposed techniques in the Ring-VCO design are effective. The output frequency range of the proposed PLL is 0.06–1.92 GHz, and the RMS jitter at 0.48 GHz and 1.92 GHz is 2.61 ps and 2.5 ps, respectively. The RMS jitter over the whole output frequency range is given in Fig. 8, which is less than 3.8 ps with a current consumption of 9.7 mA. The implementation of the wideband low-jitter PLL benefits from the high performances of the Ring-VCO which directly determine the out-band phase noise and output frequency range of the PLL.

Table I summarizes and compares some wideband low-jitter PLLs. It can be seen from Table I that the proposed PLL realizes wideband output, low jitter, and competitive figure of merit (FoM) using an old 180 nm CMOS process.

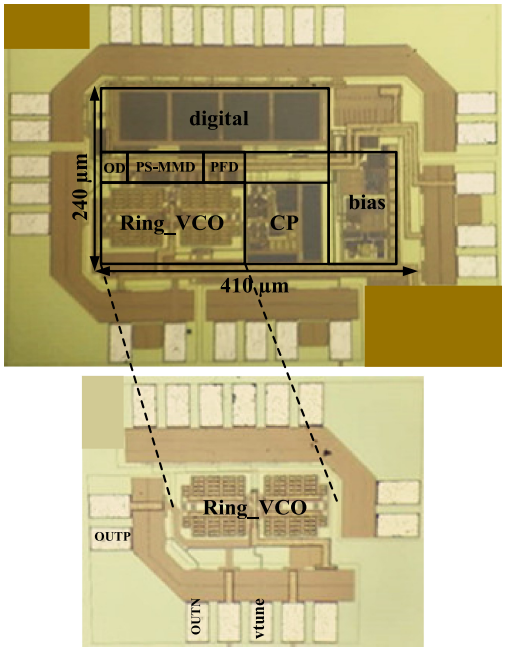

Fig. 6. Chip micrograph.

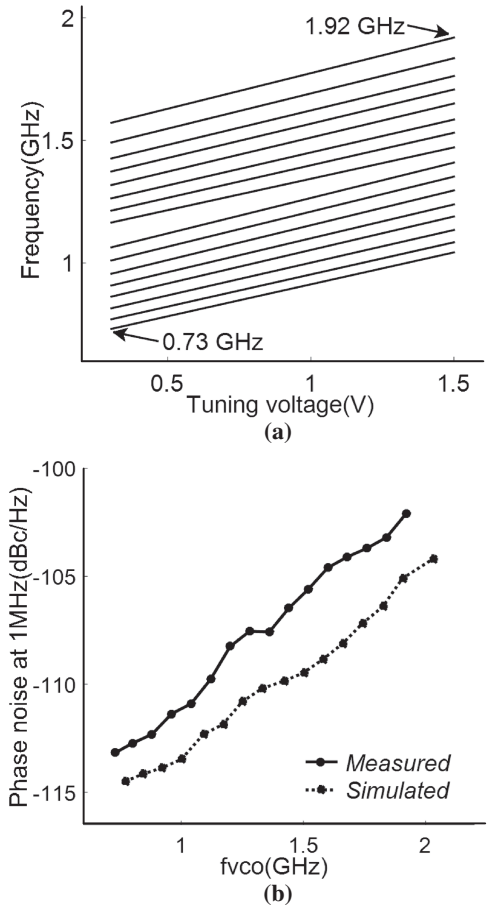

Fig. 7. The performances of the proposed Ring-VCO (a) tuning curves, and (b) phase noise.

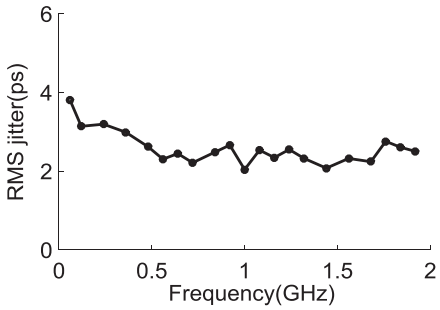

Fig. 8. The RMS jitter of the proposed PLL within the whole frequency range.

Table I. Results and comparisons.

Refs	9	14	23	This work
Process (nm)	90	65	28	180
Freq. Range (GHz)	3.5–7.1	0.25–1.65	0.032–2.0	0.06–1.92
Freq (f_o/GHz)	5	0.58	2	0.48
F_{REF} (MHz)	10	32	30	48
Jitter (ps)	3.8	4.23	19.3	2.61
Power (mW)	29.64	10.5	5.3	17.4
FoM (dB)[a]	−210.96	−217.26	−207	−219.25

[a]FoM = $10log_{10}[(\sigma)^2 \cdot (Power)]$

5. Conclusion

A topology of wideband low-jitter PLL with an optimized Ring-VCO has been presented. The proposed low phase noise wideband Ring-VCO adopts two-stage delay cells and an AMOS varactor pair is employed to improve the fine tuning linearity. Meanwhile, an additional AMOS varactor pair is utilized to reduce the K_{vco} variation in the coarse tuning process and enhance the tolerance in temperature and voltage variations. Strategies used in this paper are effective in the Ring-VCO and PLL designs. The measured output frequency of the PLL is from 0.06 to 1.92 GHz and the RMS jitter is less than 3.8 ps over the whole frequency range.

Acknowledgments

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