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LETTER

Thermal placement on PCB of components including 3D ICs

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Abstract In this letter, we propose a method for optimizing the thermal placement of heat and non-heat generating electronic components on a printed circuit board (PCB). Use a genetic algorithm to optimize the maximum temperature of the PCB and the total wire length between components. In the case that chips stacked in 3D ICs are reconfigurable, each chip construction of 3D ICs is also changed simultaneously. The temperature of each component is obtained by circuit simulation using a simple thermal circuit model. The experimental results demonstrate that the placement of components can be optimized well for lowering the maximum temperature with shorter wire lengths.

Keywords: thermal placement, 3D IC, printed circuit board, optimization, electronic component
Classification: Integrated circuits

1. Introduction

Thermal management of electronic devices has been a hot topic and challenge because of the downsizing of devices and increasing of power density. There are many thermal management approaches such as circuits and systems for lowering power consumption and structures and materials for cooling [1]. Thermal placement optimization is a thermal design technique. It is important for mobile and wearable devices in particular that components be placed so that heat is not concentrated.

The physical design stages in which placement techniques are applied are classified in mainly three categories: chip designs such as system-on-chip (SoC), package designs such as system-in-package (SiP), system-on-package (SoP), and 3D ICs, and printed circuit board (PCB) designs such as system-on-board (SoB). A technique for placing small circuits (standard cells) on a chip was developed by partitioning netlists in the 1960s. After that, simulated annealing, min-cut, and analytic techniques have been developed [2]. Optimizing placement in cell-based designs generally involves minimizing the area of cells and the power consumption due to wire capacitance. Thermal-aware floorplanning methods for VLSI have been proposed [3, 4, 5, 6, 7, 8, 9]. Thermal-aware 3D network-on-chip (NoC) designs have been proposed [10, 11]. Related to the thermal placement of 3D ICs, thermal through-silicon-via (TSV) optimization [12, 13, 14, 15, 16] and thermal floor plans [17, 18, 19, 20, 21, 22, 23, 24, 25, 26] have been presented. Placement optimization of chips in SoP designs has been presented [27]. In PCB designs, thermal placement techniques for components have been presented [28, 29, 30, 31]. For satisfying objective functions (e.g., temperature or power), genetic algorithms, ant colony algorithms, etc. have been used to optimize component locations so that temperatures are reduced.

Electronic devices have many components placed on a PCB. Integrated circuits, which are main components controlled electrically, include processors, memories (e.g., NAND flash and DDR4 SDRAM), wireless (e.g., WiFi, Bluetooth, GPS, W-CDMA, and LTE) modules, audio codecs and amps, power management ICs, and sensor (e.g., accelerometer, gyroscope, pressure, and compass) ICs. These belong to heat-generating electronic components. Passive elements such as resistors, capacitors, and inductors may be included. AUX interface components such as USB, HDMI, miniPCIs, micro SDs, SIM cards, earphones, mics, and power sources may be installed in the device body. Moreover, for mobile/wearable devices, components like speakers, antennas, cameras, switches, and batteries are incorporated in thin and small device bodies. Some of these components must be placed at predetermined positions. However, some components can be placed freely. Most technical papers regarding the thermal placement of components on a PCB handle heat-generating electronic components only [28, 29, 30, 31]. They mainly deal with the optimal thermal placement of only IC packages on a PCB. Some techniques related to wire length optimization have been reported [32, 33, 34, 35, 36]. A method for optimizing wiring and interconnection between PCB modules has been presented [32]. A solution methodology for the optimal placement problem on multichip module (MCM) considering both thermal and routing design objectives simultaneously has been presented [33]. A thermal-driven floorplanning algorithm for 3D ICs has been proposed [34]. The method can improve the wire length and maximum chip temperature in 3D ICs. Ref. [35] reduces the maximum temperature and wire congestion of 3D circuits. An efficient thermal-aware 3D floorplanner for heterogeneous multi-processor architectures has been proposed [36]. By a multi-objective evolutionary algorithm, temperature and wire length are simultaneously reduced. However, optimization of components on a PCB including reconstitution of 3D ICs has not been reported.

In this letter, we present a novel method for placing components on a PCB in consideration of heat generation. The method can handle both heat and non-heat generating

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components, the reconfiguration of chips stacked in 3D ICs, the temperatures of all components including 3D ICs on a PCB, and the replacement of components to minimize the total wire length within the allowable temperature range so that components are placed in a such a way that the maximum temperature of the components on a PCB is minimized.

The remainder of this letter is structured as follows. In Section 2, we present the proposed method for optimizing the thermal placement of components on a PCB. In Section 3, we show experimental results obtained under conditions that include prohibited areas, non-heat generating components, and reconfigurable 3D ICs. In Section 4, we discuss about the stop criterion of the algorithm. Finally, Section 5 concludes the letter.

2. Proposed optimization method

We present a method for minimizing temperature rise caused by heat generated by electronic components on a PCB. The procedure is described in accordance with the flowchart in Fig. 1.

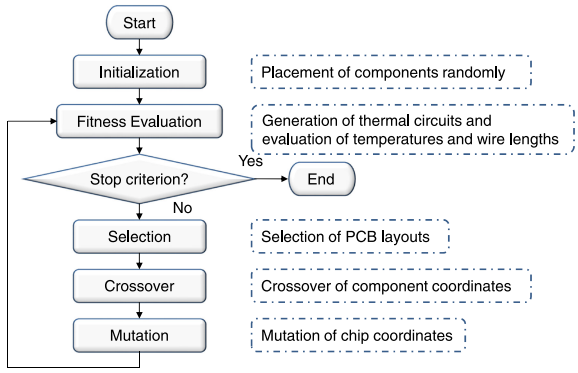

Fig. 1. Flowchart of thermal placement using genetic algorithm.

2.1 Initialization

Components are placed at random on a PCB, and their coordinates are determined. If a component does not fall within locatable areas on a PCB or overlaps with another component that has already been placed, the coordinates of the component are decided again with a random number. When components are placed, whether the chip can be stacked or not is checked by a reference table. If enabled, whether to stack the chip or not is decided randomly. If not enabled, the chip is placed somewhere else. For one individual, all components are well placed on a PCB. These operations are repeated on the basis on the number of individuals.

Chip size, power consumption, and chip-to-chip connection information are read from a reference table. The coordinates of each component and the stacking situation are stored as a PCB layout.

2.2 Fitness evaluation

The temperature and wire length of components placed on a PCB were evaluated. A thermal circuit was automatically generated from the component coordinates and stacking situation of chips. Temperatures at each position were obtained by executing a commercial circuit simulator, HSPICE.

In this work, as a thermal circuit model, a PCB area of 130 mm × 130 mm was divided into 169 small cuboidal blocks (called "thermal cells"). A thermal resistance model for three-dimensional heat flow was used as an equivalent circuit model for each cell, as shown in Fig. 2.

An illustration of an IC package with a single chip, for which a flip-chip package is assumed, is shown in Fig. 3. One chip consists of three layers: a chip substrate, which is composed of silicon, a device, which approximates the heat-generating region, and metal, which approximates a multilayer-wiring region. A 3D IC is formed by being connected with micro-bumps between chips.

Each layer (chip substrate, device, metal, flip-chip bumps, package substrate, and package bumps) in a package with a single chip or a 3D IC is expressed with one 3D resistance model. Thermal resistance for natural convection can be expressed as

$$R_T = \frac{1}{A \times HTC}, \tag{1}$$

$$HTC = 2.51 \times C \times \left(\frac{\Delta T}{L}\right)^{0.25}, \tag{2}$$

where A is the surface area, HTC stands for a heat transfer coefficient, C is the shape parameter, ΔT is the temperature difference, and L is the representative length.

There are various physical restrictions such as different chip sizes and different TSV arrangements. Chip stacking conditions can be set into a chip information table. Whether it is possible to stack chips is identified by the 3D group number of each chip.

When evaluating temperature, a value obtained by rounding the highest temperature for all components to the first decimal place was stored in the array. When evaluating wire length, wire lengths were obtained from chip coordinates and the connection ratio between chips. These evaluations were repeated for each individual. When the highest temperature was compared among individuals, the individual with a lower temperature was selected, and when temperatures were the same in terms of the allowable temperature difference, the individual with a shorter wire length was selected. The best individual among all individuals was stored as an elite individual. The objective functions are as follows.

$$\text{Minimize: } f = \max(component_i); \quad i = 1, 2, \cdots, m,$$

$$g = \sum_{j=1}^{n-1} \sum_{k=j+1}^{n} R_{jk} D_{jk}, \tag{3}$$

where f is the temperature, m is the number of components, g is the wire length, n is the number of chips, R_{jk} is the connection ratio between chips, and D_{jk} is the distance between chips.

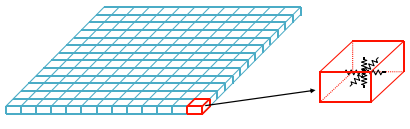

Fig. 2. Thermal resistance model for PCB.

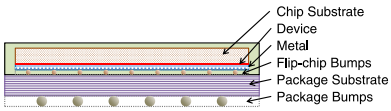

Fig. 3. Illustration of IC package.

2.3 Stop criterion

When a termination condition was satisfied, the processing was finished. The condition used in this work was when the number of iterations reaches a specified generation number. As the stop criterion, it is difficult to use the fixed values in temperature and wire length because the maximum temperature and wire length change by various conditions such as power consumption and physical layout. In practical use, using increment values in temperature and wire length may become one means. In this letter, the number of iterations was used for the stop criterion. The use of the fixed number makes the stop criterion simple, but the method may not get the optimal solution or may waste many iterations. These details are discussed in Section 4.

2.4 Selection

As a method of selection, tournament selection was used in this work. Two individuals were selected randomly among all individuals, and individuals that were better in the evaluations of temperature and length were stored. This operation is repeated on the basis of the number of individuals (50 in this work).

2.5 Crossover

As a method of crossover, blend crossover was used in this work. There were individual 1 and 2. Component A was placed into each one as shown in Fig. 4. The relationship between component A for individual 1 and component A for individual 2 is shown in Fig. 5(a). The area (blue frame) of $dx \times dy$ was decided from the center coordinates of two components. As shown in Fig. 5(b), a new area (red frame) was generated by α times both sides of the area, where α was 0.3 in this work. In the new area, component A was generated randomly, and the component was named A'. The placement of components in the next generation is shown in Fig. 6. The operation was executed for all chips and was repeated until all chips were placed.

2.6 Mutation

According to probability, mutation is performed. Each component location and the kinds of chips that were stacked were changed.

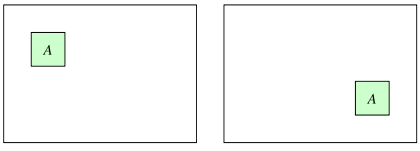

Fig. 4. Two individuals before crossover.

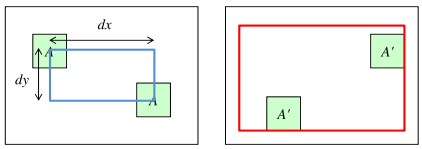

Fig. 5. New area generation for crossover. (a) Area (blue) made from centers of two components and (b) new area made by α times both sides.

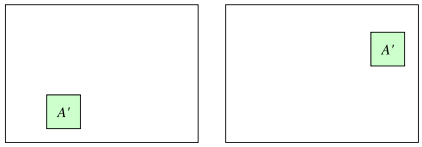

Fig. 6. Component placement in each individual after crossover.

3. Experimental results

In this section, we present experimental results obtained by using the proposed method. All processing shown in Fig. 1 was implemented in C and executed automatically.

Table I shows the conditions of the genetic algorithm used in the experiments. Table II lists information on the chips. The number of chips used was 20. The 3D group number means that chips with the same number can be stacked into one 3D IC if necessary. There are some restrictions such as chip size and TSV arrangement for chip stacking. Whether each chip can be stacked or not is recognized by the 3D group number. In Table II, the 3D group number means that the stackable chips have the same group number. For example, the chip numbers 1, 9, and 12 are the same group number 1 and their chips can be stacked. Please note that the group number 0 is not stacked with other chips. As a result, chips with different size are given to different group numbers and cannot be stacked. Although we call each part a "chip" here, it can be any component (e.g., component with power consumption of zero). Chips that 3D group number is 0 are not stacked with other chips. A chip with 0 W power means a non-heat generating component. In Table II, chip number 2 represents a non-heat generating component. Table III exhibits the normalized connection ratios between chips, which means that the closer to 1 the ratio is, the higher the number of connections.

Table I. Conditions used in genetic algorithm.

Parameter	Value
Individuals	50
Number of generations	1000
Crossover probability	0.95
Mutation probability	0.05

Fig. 7 shows the dimensions of a PCB layout with areas where placement is prohibited. The prohibited areas are used for placing predetermined components. Fig. 8(a) shows the placement of components in an initial state. For

Table II. Chip information.

Chip No.	Power (W)	3D Group No.	Size (in mm)
1	0.5	1	10×10
2	0	0	30×30
3	0.2	2	30×30
4	0.2	2	30×30
5	0.5	0	30×10
6	0.1	4	30×10
7	0.1	3	10×30
8	0.7	2	30×30
9	0.5	1	10×10
10	0.5	0	10×10
11	0.2	4	30×10
12	0.1	1	10×10
13	0.7	2	30×30
14	0.2	2	30×30
15	0.4	3	10×30
16	0.8	2	30×30
17	0.2	3	10×30
18	1.2	2	30×30
19	0.3	4	30×10
20	0.7	2	30×30

Table III. Normalized connection ratio (numbers of 1 to 20 represent a chip number).

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	-	0.6	0.7	0.5	0.3	0.5	0.6	0.2	0.9	0.1	0.2	0.7	0	0.9	0.3	0.6	0	0.6	0.2	0.6
2		-	0.7	0.9	0.2	0	0.2	0.3	0.7	0.5	0.9	0.2	0.2	0.8	0.9	0.7	0.3	0.6	0.1	0.2
3			-	0.9	0.4	0.7	0.8	0.4	0.5	0	0.3	0.6	0.1	0	0.6	0.3	0.2	0	0.6	0.1
4				-	0.6	0.5	0.6	0.9	0.3	0.7	0.4	0.5	0.2	0.5	0.4	0.7	0.4	0.4	0.3	0
5					-	0.4	0.3	0.1	0.4	0.9	0.2	0	0.6	0.8	0.9	0.2	0.6	0.6	0.4	0.9
6						-	0.7	0.2	0.7	0.2	0.2	0.6	0.1	0	0.6	0.1	0.5	0.9	0.4	0.9
7							-	0.5	0.9	0.7	0.7	0.6	0.7	0.3	0.6	0.5	0.6	0.3	0.9	0.4
8								-	0.8	0.5	0	0.9	0.6	0.3	0.8	0.5	0.6	0.1	0.1	0.5
9									-	0.4	0.4	0.4	0.7	0.6	0.3	0.1	0.7	0.5	0.9	0.6
10										-	0.9	0.7	0.5	0.3	0.8	0.8	0.3	0.1	0.8	0.9
11											-	0.8	0.9	0.7	0.7	0.6	0.4	0.3	0	0.3
12												-	0.2	0.4	0.7	0.7	0.5	0.4	0.8	0.1
13													-	0	0.8	0.5	0	0.6	0.4	0.6
14														-	0.9	0	0.8	0.1	0.3	0.1
15															-	0.5	0.6	0.6	0.4	0
16																-	0.6	0	0.2	0.7
17																	-	0	0.4	0.8
18																		-	0.8	0.3
19																			-	0.2

example, component *C* shows that chip numbers 3 and 16 were stacked into a 3D IC. Fig. 8(b) shows the placement of components after performing the proposed optimization. For example, we can see that component *C* was changed to a 3D IC of chip numbers 3, 4, and 18. In Figs. 8(a) and 8(b), component *B* is a non-heat generating component because it is composed of chip number 2 (the power is 0 W and it is not stacked with other chips). Fig. 9 shows changes in the total wire length. The wire length is the value obtained by multiplying the distance between chips in millimeters by the coefficient in Table III, and no unit of quantity required. As the number of generations increased, the total wire length became shorter. The length became almost constant from about 600 generations.

Fig. 10 shows the power consumptions of each component, where (a) is the result for the initial state and (b) that after optimization. In the initial state, the number of components was 11 (*A* to *K*). After optimization, the number became 16. Each number in the figures corresponds to the chip number in Table II.

Fig. 11 shows the temperatures of each component, where (a) is the result for the initial state and (b) that after optimization. The simulation results obtained by using the simple thermal model were in good agreement with those obtained by the commercial thermal solver [37]. When the

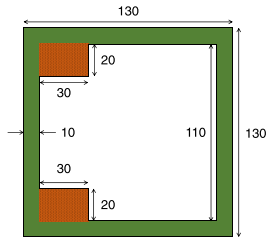

Fig. 7. Dimensions (in mm) of PCB layout with two areas where placement was prohibited.

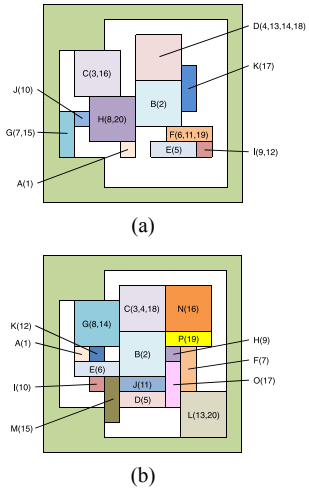

Fig. 8. Placements on PCB: (a) in initial state and (b) after being optimized.

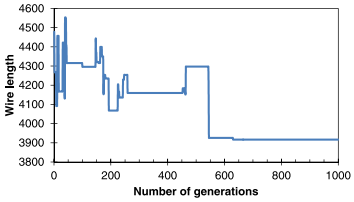

Fig. 9. Total wire length on PCB to number of generations.

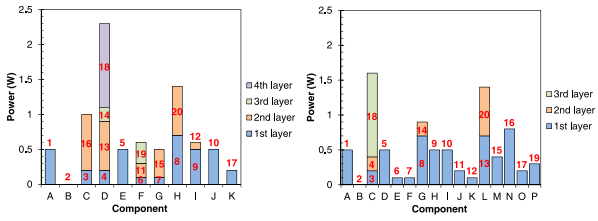

Fig. 10. Power consumptions of each component: (a) before and (b) after optimization. Red numbers represent each chip number.

component power consumptions shown in Fig. 10 were high, the temperatures of the components were not always high, as shown in Fig. 11. Each component temperature was decided by the power density of heat generation and the surrounding situation. A thermal resistance model is applied to component *B* as well as other heat generating components. This means that the thermal resistance models of both non-heat generating components and heat generating components are used for thermal simulations. Fig. 12 demonstrates temperature distributions before and after optimization. We can see that the maximum temperature went down.

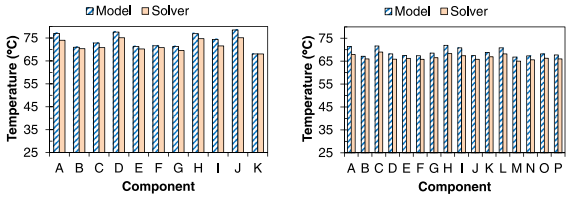

Fig. 11. Temperatures of each component: (a) before and (b) after optimization.

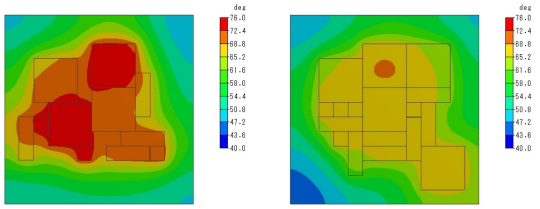

Fig. 12. Thermal distribution on PCB: (a) before and (b) after optimization.

4. Discussion

We used the maximum number of generations for the stop criterion of the optimization algorithm in this letter. We here discuss the possible problems by setting the fixed iteration number. Fig. 13 shows the maximum temperature and total wire length to the number of generations. The results are different from those described in Section 3 because of results obtained by re-executing. The maximum number of generations was 2,000. The changes in temperature and wire length are converged at about 1,000 iterations. Although it depends on the conditions of the optimization problem, it is possible to converge at about 1,000 iterations under the condition used in this letter. If the number of iterations is smaller (e.g., 500), the temperature and wire length do not converge. If the number of iterations is larger (e.g., 2,000), 1,000 iteration steps become a waste. For this reason, the number of iterations was set to 1,000 times in the experiment of Section 3. However, it should be noted that the number of iterations for convergence varies depending on the conditions. For practical use, although an evaluation function with temperature and wire length should be used for the stop criteria, it will be the future work.

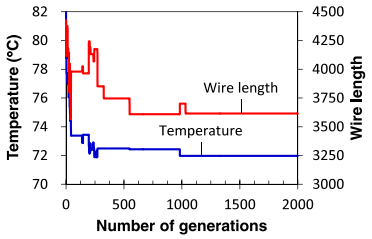

Fig. 13. Changes in temperature and wire length.

5. Conclusion

In this letter, a method for optimizing the thermal placement of electronic components on a printed circuit board was presented. The method can be performed by obtaining temperatures with a simple thermal circuit model, reducing the maximum temperature with a genetic algorithm, and shortening the total wire length. In addition, the method not only moves the positions of components but can also change the construction of stacked chips in 3D ICs.

Acknowledgments

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