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LETTER

Study on the single-event upset sensitivity of 65-nm CMOS sequential logic circuit

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Abstract This study uses a pulsed laser to investigate the sensitivity of a sequential logic circuit to a Single-Event-Upset (SEU) under different supply voltages, clock frequencies, and circuit architectures. The experimented sequential logic circuit is a D flip-flop chain manufactured in 65-nm bulk CMOS technology. The results indicate that as the voltage decreases, the SEU sensibility of the circuit increases, and in particular at low voltage ranges, it increases significantly. Additionally, the effect of clock frequency on the sensitivity of the sequential logic circuit is mainly related to the propagation of Single-Event-Transients (SETs) that are generated in combinational logic circuits. It was also found that, the Set-architecture circuit is more sensitive to SEUs during the data "0" test, while the Reset-architecture circuit is more sensitive to SEUs during the data "1" test. In addition, the failure mechanisms of SEU induced by Set-structure and Reset-structure are revealed using SPICE simulations.

Keywords: pulsed laser, single-event-upset (SEU), voltage, frequency, circuit architecture

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

The Single-Event-Upset (SEU) effect is one of the main radiation effects that cause the failure of semiconductor devices in space environments [1, 2, 3]. The failure may occur when the sensitive node of a semiconductor device is struck by a single high-energy particle in space [4]. In recent times, there has been a sharp reduction in device supply voltage as technology nodes are scaled down, which could make integrated circuits (ICs) more sensitive to SEUs.

Master-slave flip-flop (FF), a typical sequential logic circuit, is extensively used in modern integrated circuit designs. These FFs may be upset if (1) a particle strikes on a master or slave trigger and deposits charge exceeding the critical charge (Qcrit) [5, 6] during the period of latch hold, or (2) a single-event-transient (SET) generated on the master-trigger hit by a particle propagates to the slave-trigger during the latching period [7, 8, 9]. Additionally, the combination logic may also generate SETs, which could be captured by the latching units and cause an SEU.

Currently, many studies have focused on the influence factor of the SEU sensitivity of sequential logic circuits. For example, C.H. Chen et al. studied the effects of supply voltage and frequency on the SEU sensitivity of 65-nm DFF circuits using alpha irradiation [10], and R.M. Chen researched the effect of these factors on 40-nm DFF circuits by heavy ions [11]. Mahatme et al. studied the relative contribution of different logic elements to the overall single-event error rates and indicated that the upset caused by the combinational logic circuit is dominant when the clock frequency is high [12]. Therefore, it is important to analyze the impact of different combinational logic elements on the SEU sensitivity of FF circuits. However, the influence mechanism of SEU sensitivity of sequential logic circuits has not been clearly revealed. In addition, the SEU sensitivity of a circuit would change if the structure and function in a sequence circuit changed [13]. As far as the authors are aware, the effect of the Set-architecture and Reset-architecture in a D-type Flip-Flop (DFF) chain on the SEU sensitivity of a device has not been reported yet, and this will be studied in this paper.

Although ground-based heavy ion testing is the predominant methodology for testing single event effects (SEEs), it is scarce and time-consuming [14]. Pulsed laser-induced SEE testing has become a popular technique since it can use table-top laser systems to perform charge injection into devices through photon absorptive processes [15, 16, 17, 18]. In this study, the effects of voltage, frequency, and circuit architecture on the SEU sensitivity of circuits are experimentally investigated using a pulsed laser. The impact mechanisms of these factors on the SEU characteristics are discussed and analyzed using a simulation program with integrated circuit emphasis (SPICE) simulation.

The remainder of this paper is organized as follows: Section II describes the design of the chip; Section III introduces the experimental setup of a pulsed laser; Section IV presents the experimental results of devices irradiated by a pulsed laser; Section V presents a discussion on the experimental results; and Section VI draws the conclusions of this study.

2. Test chip design

The test chip, which contains six DFF chains, was designed and manufactured using 65-nm bulk CMOS technology, as shown in Fig. 1. Each DFF chain consists of 2000 stage shift register. Table I outlines the different details of the DFF chains. As it can be seen, the DFFB chain does not have Set-architecture and Reset-architecture in the structural design, while the DFFRS, DFFRS_INV, and DFFRS_INVH chains have them. The Set-architecture and Reset-architecture were

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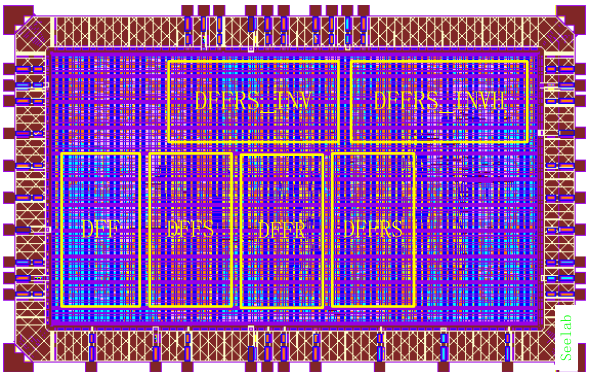

Fig. 1 Test chip layout

Table I Details of DFF chains.

FF Chain	Set-architecture	Reset-architecture	20 Inverters	Hardened
DFFB	No	No	No	No
DFFR	No	Yes	No	No
DFFS	Yes	No	No	No
DFFRS	Yes	Yes	No	No
DFFRS_INV	Yes	Yes	Yes	No
DFFRS_INVH	Yes	Yes	Yes	Yes

adopted by DFFS chain and DFFR chain, respectively. The DFFRS_INV and DFFRS_INVH chains contain also 20 inverters in front of the Set-architecture and Reset-architecture of each DFF unit, and a hardened design is carried out [19] to mitigate SETs in front of the Set-architecture, Reset-architecture, and Clock-architecture of the DFFRS_INVH chain. Since the pulsed laser cannot penetrate the multilayer metal layer, the back of the device was exposed before starting the experiment, in order to enable the pulsed laser to effectively enter the chip [20, 21].

3. Pulsed laser experiments

The experiment was carried out on a pulsed laser single-event-effect facility at the National Space Science Center (NSSC) in China. The key parameters of the pulsed laser are as follows: wavelength ~1.064 μm, pulse width ~20 ps, spot size ~2-3 μm, pulse repetition frequency ~1-50 kHz, and equivalent linear energy transfer (LET) ~0.1-200 MeV·cm^2/mg [22]. The block diagram of the experimental setup and an image of the experimental setup during the experiment are shown in Fig. 2 and Fig. 3, respectively. The device under test (DUT) was mounted on a test board. The test board system could detect errors and output the error counts to a computer using USB. The test modes and frequencies could be configured by the software and the voltage could be altered by adjusting the load resistor on the test board. A power supply voltage of 1.2 V was selected for the experiment. At room temperature, the SEU characteristics of the D flip-flop chains were tested for clock frequencies of 0.625 MHZ, 2.5 MHz, 10 MHz, 20 MHz, and 40 MHz. In addition, the SEU sensitivity of the D flip-flop chains with a voltage range from 1.0 V to 1.4 V was also tested.

The SEU sensitivity of a shift register is represented by the SEU cross-section, which can be calculated as:

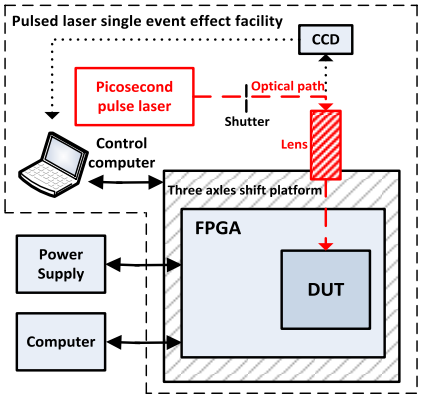

Fig. 2 Principle block diagram of the experimental setup.

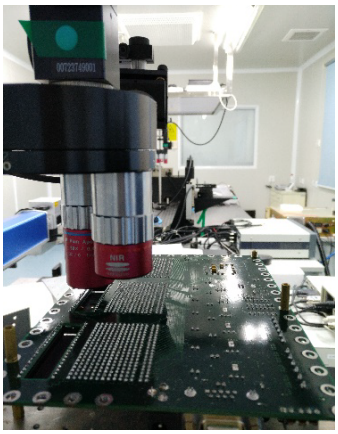

Fig. 3 Image of the experimental setup during the experiment.

$$\sigma = \frac{n}{F * N}$$

where n is the number of measured single-event upsets, F represents the total fluence and is defined as the number of injected laser pulses per cm^2 during testing, and N is the stages-number of flip-flops in the shift register chain.

4. Experimental results

4.1 Effect of voltage

The SEU cross-section of the DFFRS chain in Fig. 4 shows that when the supply voltage decreased from 1.4 V to 1.0 V, the SEU cross-section increased. When the voltage changed from 1.4 V to 1.2 V, the SEU cross-section increased linearly from 4× 10^{-6} to 3.6× 10^{-5} cm^2/stage. It is worth noted that when the voltage decreased from 1.2 V to 1.1 V, the SEU cross-section increased dramatically from 3.6× 10^{-5} to 1.72× 10^{-3} cm^2/stage. It can be concluded that, at higher voltage levels, the relationship between SEU cross-section and voltage is linear, while at lower voltages, the SEU sensitivity of the DFFRS chain increases sharply with the decrease of voltage.

4.2 Effect of frequency

The SEU cross-section of the DFFRS, DFFRS_INV, and DFFRS_INVH chains as a function of the clock frequency is shown in Fig. 5, where an optimized curve fitting was conducted based on the data points. As it can be seen, the

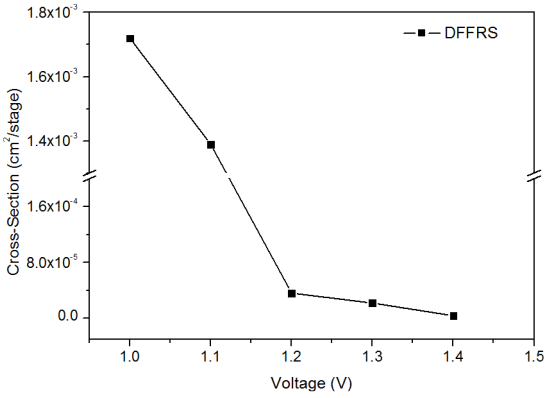

Fig. 4 SEU cross-section of the DFFRS chain versus the supply voltage.

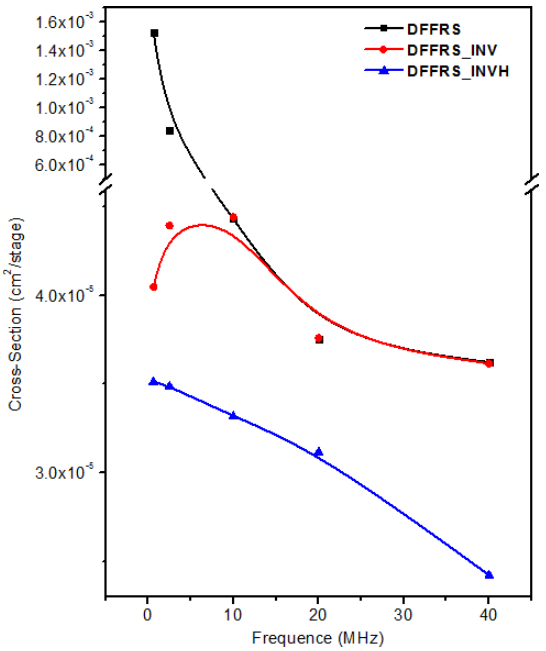

Fig. 5 SEU cross-section vs. frequency of the DFFRS, DFFRS_INV, and DFFRS_INVH chains.

SEU cross-section decreased for all three chain types when the frequency increased from 0.625 MHz to 40 MHz. However, only the DFFRS_INVH chain demonstrated a linear decrease with increasing frequency. Besides, the rate at which the SEU cross-section of the DFFRS chain decreased became slower as the frequency increased. At lower frequencies, the cross-section of the DFFRS_INV chain was significantly smaller than that of the DFFRS chain. However, both SEU cross-sections were nearly identical at higher frequencies. Moreover, as the frequency increased, the SEU cross-section of the DFFRS_INV chain increased first and then decreased. The turning-point frequency was about 5 MHz and the peak value of the SEU cross-section was approximately 4.44×10^{-5} cm^2/stage. In the range between 0.625 MHz and 40 MHz, the cross-section of the DFFRS_INVH chain was always smaller than that of the DFFRS_INV chain.

4.3 Effect of circuit architecture

Fig. 6 shows the SEU cross-section of the DFFB chain and the DFFRS chain for a data "0" and data "1" test under different laser energies. It can be directly inferred from the

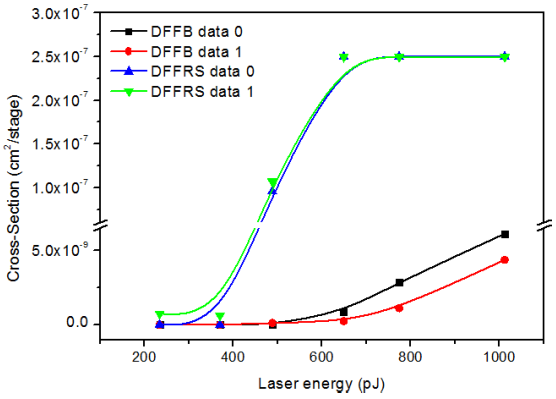

Fig. 6 SEU cross-section vs. laser energy of the DFFB and DFFRS chains in data "0" and data "1" tests.

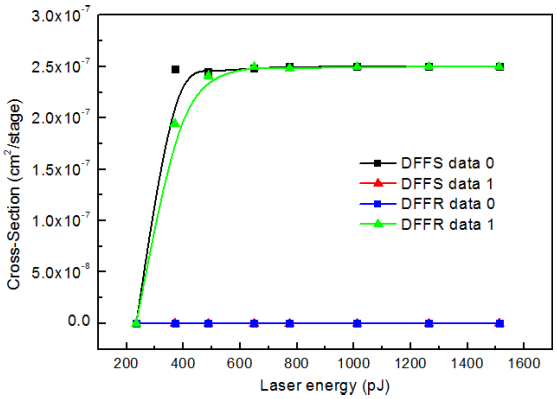

Fig. 7 SEU cross-section vs. laser energy of the DFFS and DFFR chains in data "0" and data "1" test.

SEU threshold and the SEU cross-section that the DFFRS chain was very sensitive to SEU. Fig. 7 shows the results of the DFFS and DFFR chains. It can be seen that the DFFS chain demonstrated almost no upset in the data "1" test. In the data "0" tests, the upset of the DFFS chain occurred at a laser energy of 370 pJ, and the SEU cross-section was subsequently saturated. As opposed to the DFFS chain, the DFFR chain was greatly susceptible to upsets in the data "1" test, while it demonstrated very low sensitivity in the data "0" test. In conclusion, the Set-architecture circuit causes higher sensitivity to the "0" test and lower sensitivity to the "1" test, while the Reset-architecture circuit results in higher sensitivity to the "1" test and lower sensitivity to the "0" test. When the Set-architecture and Reset-architecture are used in one circuit, this circuit may show a higher SEU sensitivity to both the "0" and "1" tests.

5. Discussion

5.1 Voltage dependence

When an energetic particle strikes a sensitive location (typically the reverse-biased drain junction of a transistor biased in the "off" state), the charge collected by the junction results in a transient current in the struck transistor [23, 24]. Current flows through the load transistor, therefore inducing a voltage drop at its drain. If the amount of charge collected at a sensitive node exceeds the Qcrit, a circuit upset may occur. Qcrit is usually defined as the minimum amount of

charge collected at a sensitive node required to cause a circuit upset. The value of Qcrit is proportional to the product of the voltage and the node capacitance [25]. In general, the nodal capacitance of a device at room temperature will be constant. Therefore, the SEU cross-section increases linearly when the voltage decreases, which is consistent with the experimental results at higher voltage ranges.

The decreases in voltage will enhance the horizontal diffusion of carriers and increase the sensitive area of the devices [26]. Additionally, at higher voltage, the off-NMOS is the most sensitive transistor, while the PMOS may become sensitive when the voltage decreases, which further increases the sensitive area of the device. Therefore, a slight variation of low power supply voltage may cause a worse case in a circuit.

5.2 Frequency dependence

In this paper, three mechanisms that may cause SEU in Flip-Flop were introduced. In the first condition, if the collected charge in the latching unit exceeds the Qcrit, it will result in a "direct-latch-upset". In the second condition, a SET generated at the master stage can propagate to the slave stage during the latching period and cause an upset, which will result in an "internal-SET-induced-upset". In the third condition, a SET generated by combinational logic outside the DFF unit in the circuit may be captured by the FF and cause an upset, which will cause an "external-SET-induced-upset". This work was mainly focused on the SET-induced-upset since the direct-latch-upset is independent of frequency [11].

The DFFRS_INV chain demonstrates better performance than DFFRS at lower frequencies, due to the additional 20-stage inverters in front of the Set and Reset terminals. The 20-stage inverters increase the delay in the external combinational logic circuit and filter out SETs generated by the external circuit, decreasing the number of external SET-induced-upsets. The filtering ability of the 20-stage inverters weakens as the clock frequency increases, making the circuit more sensitive to SEUs. Therefore, the filtering effect dominates at lower frequencies. However, at higher frequencies, the filtering effect of the external combinational logic circuits has almost no effect on the SEU sensitivity of the circuits.

The DFFRS_INVH and DFFRS_INV chains have the same circuit architecture, while the DFFRS_INVH chain adopted measures to mitigate SETs in front of the Clock, Set, and Reset terminals. The amount of SETs generated in the external combinational circuit will decrease due to this hardened design. Therefore, compared to the DFFRS_INV chain, the SEU sensitivity of the DFFRS_INVH chain is small since it generates less external-SET-induced upsets. Hence, the impact of frequency on the SEU sensitivity of the DFFRS_INVH chain may be mainly related to internal-SET-induced upsets. The parameters related to internal SET-induced-upsets for DFF have been given in detail in [27]. The probability that an SEU generated in the front-stage FF propagates to the later-stage FF can be expressed by the following equation:

$$\eta = \frac{T_{wov}}{T_{clk}} = \frac{T_{clk} - (T_{clk_q} + T_{logic} + T_{setup})}{T_{clk}} = 1 - T_{mask} F_{clk} \quad (1)$$

where T_{wov} is the length of time that an SEU generated in the front-stage FF is captured by the later-stage FF, T_{clk} represents the clock period of the circuits, T_{clk_q} represents the delay in the output signal after the front-stage FF is triggered by an effective clock, T_{logic} represents the delay of signals in the combinational logic circuits, T_{setup} represents the setup time of the post-stage FF, and F_{clk} represents the clock frequency of the circuits. This formula has also been referred to as the timing vulnerability factor (TVF) in [28]. T_{clk_q}, T_{logic} and T_{setup} are related to the structural design of the circuit, and to operating conditions, such as the temperature and the voltage. The above formula indicates that the TVF value will decrease linearly as the operating frequency increases. This theoretical relationship confirms the linear relationship between SEU cross-section and frequency in the DFFRS_INVH chain.

5.3 Circuit architecture dependence

In a DFF chain, the function of the Set-architecture, labeled by SDN in the circuit diagram, is to set the output data to "1", and the function of the Reset-architecture, labeled by RDN in the circuit diagram, is to reset the output data to "0". Fig. 8 shows a circuit architecture diagram with a Set or Reset function. It can be seen that when a signal enters an SDN or RDN node, the signal will pass through two inverters. In order to further investigate the effect of introducing the Set-architecture and Reset-architecture design to the D flip-flop chain on the SEU sensitivity of the circuit, a SPICE simulation was performed based on the library parameters provided by the manufacturer. A DFF chain with set/reset function, which consisted of 10 stages DFF to save computational time, was modeled using SPICE. The Set/Reset function in DFF would be triggered when the signal of Set/Reset turned from "0" to "1". In the simulation, a double exponential current source [29, 30, 31] was injected into the SDN1 or RDN1 node to simulate the process of SEE occurrence.

Fig. 9 shows the simulation results of the SDN nodes and output nodes of the first, second, and last (end) stage FF when a pulse is injected at the SDN1 node position. In the data "0" test, the pulse caused the current DFF unit to upset and form a SET pulse in the inverter chain, which propagated to subsequent SDN nodes. As shown in Fig. 9, the duration of the upset data of the FF chain exceeded 9 clock periods, which was much longer than the clock period. Therefore, the propagation of wrong data to the output of the circuit is almost inevitable. The transmission of this SET pulse in

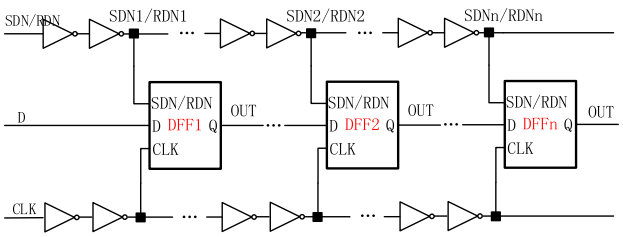

Fig. 8 Circuit structure diagram of the DFF chain.

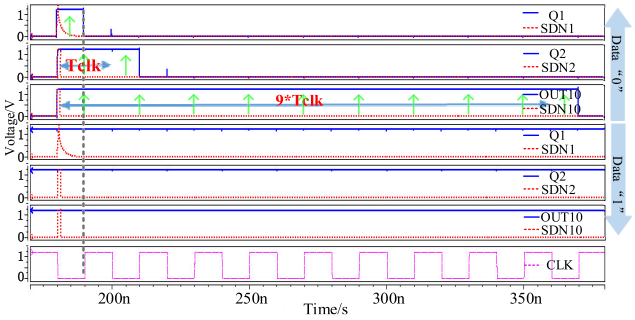

Fig. 9 Simulation results of injecting a pulse into the SDN node.

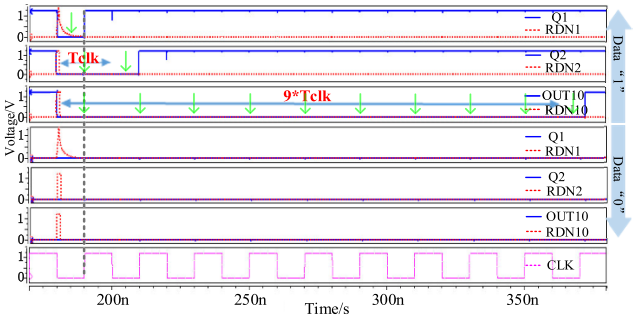

Fig. 10 Simulation results of injecting a pulse into the RDN node.

the inverter chain was considered to be an effective "set" signal and set all subsequent FF units to "1", causing almost all trigger units to flip, which greatly increased the SEU sensitivity of the circuit. In the data "1" test, when the pulse was injected into the SDN1 node, a SET pulse was also formed in the SDN2 node and propagated to subsequent SDN nodes. However, the SEU cannot be triggered by the injected transient pulse due to that the state of the circuit was data "1".

Fig. 10 illustrates the simulation results when the pulse was injected into the RDN node position. In this case, when the input data is "1", the successful propagation of the transient induced by the injected pulse in the inverter chain will cause all subsequent FF units to be reset "0", whereas the false reset signal caused by the injected pulse will be invalid when the input data is "0".

The above simulation results were almost consistent with the experimental results. Moreover, the propagation mechanism of transients induced by SEE in the combinational circuit was revealed. A 2000-stage FF chain includes a 4000-stage inverter chain. If a SET is generated in the inverter chain, the SET will propagate through the chain of the 4000 inverters, which may cause all subsequent FF units to be set or reset. This mechanism explains why the errors in the circuits demonstrate an obvious increase when Set-architectures and Reset-architectures are used in a circuit.

6. Conclusion

In this paper, a pulsed laser experiment was performed to study the effect of key factors, such as supply voltage, clock frequency, and circuit architecture, on the SEU sensitivity of a 65-nm CMOS sequential logical circuit with D flip-flop chains. The study shows that the SEU sensitivity of circuits is greatly affected by the voltage, and particularly at lower voltage levels, the SEU sensitivity of the circuit increases significantly, which should be further concerned. The results also show that, at low frequencies, the SEU sensitivity of circuits is mainly affected by external SET-induced-upsets, while at high frequencies, it is more significantly affected by internal SET-induced-upsets. Additionally, changes in circuit architecture may result in other mechanisms that may cause circuits to flip. As described in this paper, in order to perform a Set/Reset function, a large-scale combinational logic circuit was designed in a sequence circuit. However, this circuit was vulnerable to SEU and may result in function failure of the Set and Reset. The sequential logical circuit with Set- and Reset-architecture is very sensitive to SEU, so a hardened design should be considered in sequential logic circuits.

Acknowledgments

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