

LETTER

A charge recycling stacked I/O in standard CMOS technology for wide TSV data bus

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Abstract This paper describes theoretical approach and proposed scheme of wide data bus architecture using charge-recycling and stacked I/O for signal transmission via TSV (Through Silicon Via). This data bus is assumed for vertical stacked chips of 3D integration. This theoretical approach is based on probability calculation for data stream on pure random pattern. Through the calculation, power reduction ratio to normal data bus (non-charge recycling) is clarified in given conditions for power estimation in early design stage. The proposed scheme for data and clock transmission adopts Local Voltage Stabilizer (LVS) and compact level shifter for capacitor area and clock power reduction. Simulation results show that the proposed 2 story data bus architectures of 64 bits (32×2) and 128 bits (64×2) achieve competitive power efficiency (0.160 pJ/bit) with smaller size (44% to prior work) and normal operation voltage (1 V). These achievements are in dense TSVs (40 μm pitch), standard 65 nm process technology and PRBS9 data stream.

Keywords: signal transmission, charge recycling, stacked I/O

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

Because of slow down of technology scaling [1, 2, 3, 4] and several limitation of interconnect performance improvement [5, 6, 7, 8, 9, 10], three dimensional (3D) integration technology has been considered as a solution to boost system performances by tight connection between stacked chips, e.g. a processor and memories [11, 12, 13, 14, 15]. An essence to obtain higher system performance by TSV utilization is a large number of parallel interconnection between the stacked chips [16, 17, 18, 19, 20]. This parallelism has a possibility as shown in Fig. 1 to realize considerably higher data bandwidth beyond 1 Tbit/sec.

On the other hands, high bandwidth data transmission through wide data bus causes power crisis in dense packaging of multiple chips, and power reduction in data transmission should be carefully considered simultaneously in such 3D packaging.

In order to reduce the power dissipation of data transmission on wide data bus, several approaches are disclosed, e.g. lowering I/O voltage [20], charge-recycling on differential I/O [21, 22, 23] or parallel I/O [24]. However, [22] needs excessive low voltage (0.14 V) and needs sophisticated regulator. [21, 22, 23] need equalizing period for charge recycling to complement or adjacent transmission line, then high bandwidth of Gbit/sec class can not be achieved. For higher bandwidth with charge recycling, stacked I/O architectures have been disclosed [25, 26]. As shown in Fig. 2, the Stacked I/O [25, 26] has 2-story configuration (4 × 2) and realizes Gbit/sec class data transmission by fast charge transfer from top to bottom I/O via intermediate voltage node (V_{REG}).

As for [26], it is difficult to apply to 3D integration due to necessity of level conversion in the middle of TSV. The charge recycling on simple stacked I/O [25] is seemed to be the most suitable scheme to reduce power dissipation of data transmission on wide TSV data bus in 3D chip packaging.

To apply Sacked I/O scheme [25] to wide TSV data bus, there are some difficulties as listed below.

- The stacked I/O cell [25] is too large for wide data bus due to capacitance allocation for intermediate voltage.
- Clock line is out of the I/O stacking and needs full

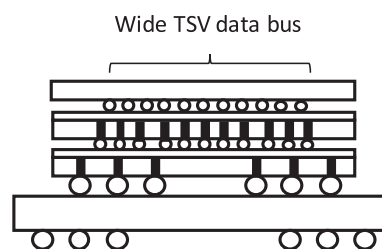


Fig. 1 3D chip packaging using through silicon vias

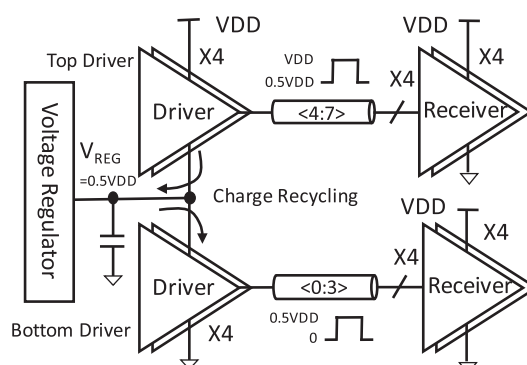


Fig. 2 Stacked I/O for charge recycling [25]

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swing, therefore clock transmission consumes much more power compared to the data transmission.

- Trench capacitors are used for larger capacitance, and it restricts process variation and requires additional cost.

This paper proposes data transmission scheme using compact Stacking I/O for wide data bus. It covers low power clock transmission with unique level shifter and calculation formula for charge recycling probability in given number of data bus width.

2. Charge recycling for wide data bus

2.1 Applicability to wide data bus

A concept of charge sharing between regulator node capacitance (C_{REG}) and TSV load capacitance (C_L) is depicted in Fig. 3. When C_{REG} is quite larger than C_L , i.e. M (a ratio of C_{REG} and C_L) is much greater than 1, then charge from the top driver can be completely utilized on the bottom driver and power dissipation can be reduced to be half ($1/2$) compared to normal 0.5VDD data swing bus. However, M is actually not so large number in wide data bus. Assuming wide data bus of more than 256 bits, realistic M is about 2.5 considering area impact and normal process (non-trench capacitor) on semiconductor chip. It means regulator voltage (V_{REG}) has $\pm 0.14VDD$ ($= 140\text{ mV}@1\text{ V VDD}$) distortion at each data cycle. This situation is not acceptable due to performance degradation of drivers. Due to above reason, [26] adopts trench capacitor with paying additional cost.

2.2 Local voltage stabilizer

To compensate small capacitance on V_{REG} , we allocate Local Voltage Stabilizer (LVS) on each pair of Top and Bottom Drivers. The LVS has common gate amplifier (Mpt, Mnt, Mpd, Mnd) and pull-up/down transistors (Mp, Mn) as shown in Fig. 4. The common gate amplifiers are biased by Common Bias Generator for gate voltage of pull-up/down transistors (Mp, Mn) to be $0.75V_{DD}$ and $0.25V_{DD}$ respectively. In initial state, Mp and Mn are basically off because of $V_{GS} < V_{TH}$, and very small DC current ($< 5 \mu A$) flows through MP and Mn. When V_{REG} goes up through charge injection from Top Driver, Mpd becomes on and drives Mn for fast pull-down of increasing V_{REG} . Meanwhile, when V_{REG} goes down by discharge to Bottom Driver, Mnt turns on and enables Mp to suppress V_{REG} decrease.

Fig. 5 shows actual layout of driver unit, which includes

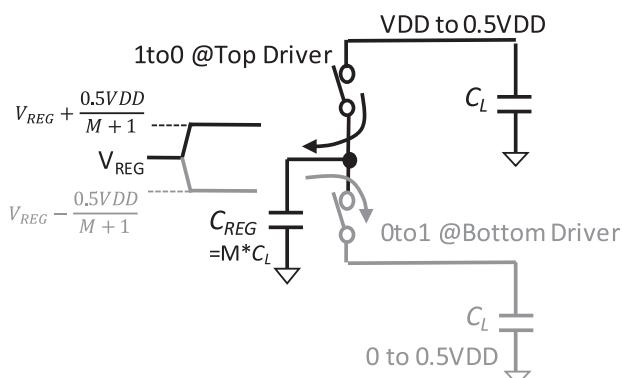


Fig. 3 Charge recycling model and V_{REG} distortion

pre-driver, driver and LVS for both floors (Top and Bottom). The size of the driver unit is $40\mu\text{m} \times 12.56\mu\text{m}$ by 65 nm SOTB process. C_L is assumed to be around 0.8 pF. Each capacitor of PMOS and NMOS has approximately 1 pF, which is about 1.25 times to C_L .

Fig. 6 shows simulation waveforms for 1×2 bit data bus configured by single driver unit. A supply voltage is 1V and data rate is 1 Gbit/sec considering non-clock recovery system.

As shown in this figure, V_{REG} distortion is suppressed within $\pm 50 \text{ mV}$ thanks to LVS. This symptom appears in wider bit bus, e.g. $4 \times 2 \text{ bits}$, $8 \times 2 \text{ bits}$... etc., because single driver unit has own LVS and the suppression of the V_{REG} distortion is basically concluded in the single driver unit basis.

Because LVS can reduce V_{REG} distortion as stated above, V_{REG} voltage returns to initial value ($0.5V_{DD}$) within almost single data cycle. However LVS needs additional power consumption due to prompt charge feed to V_{REG} node in case that charge recycling is not executed in single data cycle. The additional power consumption on LVS is severe

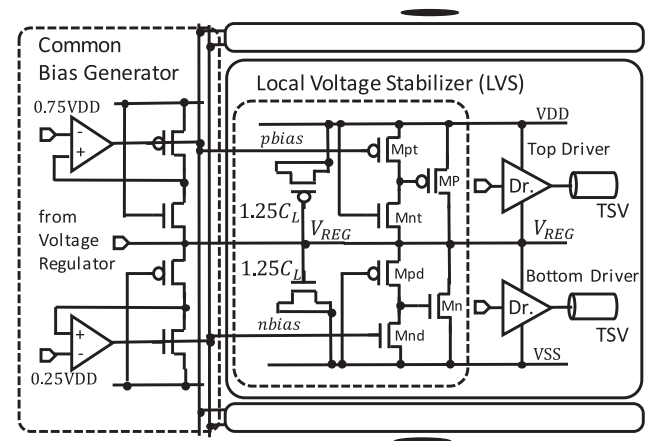


Fig. 4 Local voltage stabilizer and common bias generator

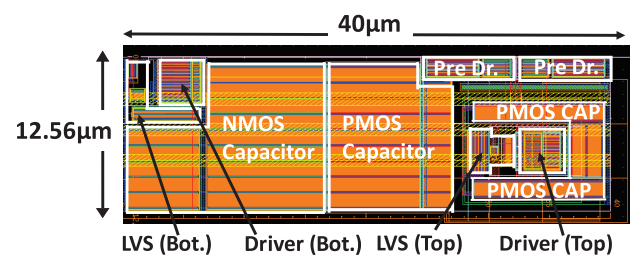


Fig. 5 Layout of driver unit

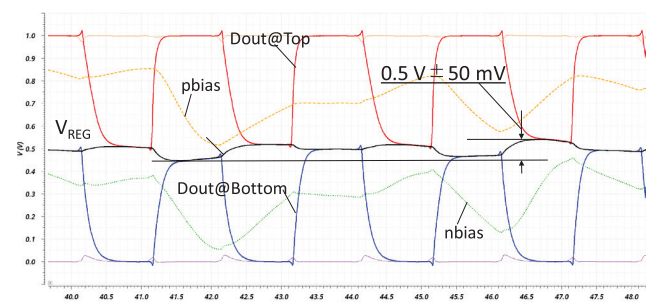


Fig. 6 Simulation waveforms of 1×2 bit data bus

disadvantage to large V_{REG} capacitance scheme [25], but it can be compensated by parallel charge sharing on wide data bus.

3. Efficiency calculation for wide data bus

3.1 Precondition

As stated above, V_{REG} behavior completes in single cycle with or without charge recycling. Therefore, charge recycling can be possible only in case of simultaneous occurrence for following 2 events;

- 1 to 0 data state transition at Top I/O
- 0 to 1 data state transition at Bottom I/O

Considering this manner, power reduction ratio can be calculated by the charge recycling probability. In this calculation, pure random pattern is assumed, and appearance probabilities of all data polarities are quite same.

3.2 Calculation example at 2×2 bits stacked data bus

At first, we are going to try to calculate an appearance probability at 2 bit data bus (#1 and #2) on Top and Bottom I/O respectively, i.e. 2×2 bits stacked data bus assuming pure random data pattern. In Table I, all cases of '0 to 1' transition are listed for 2 bits data bus. As listed in Case 1 to 6 on the table, the number of combinations for '0 to 1' transition at 1 bit on Bottom I/O can be calculated as

$${}_2C_1 \times 3^{(2-1)}. \quad (1)$$

When both bits (#1 and #2) become '0 to 1' simultaneously (Case 7 in Table I), the number of combinations for '0 to 1' transition at 2 bit on Bottom I/O can be calculated as

$${}_2C_2 \times 3^{(2-2)}. \quad (2)$$

By applying same thought to Top I/O, the number of combinations for '1 to 0' transition at 2 bit on Top I/O can be calculated as

$${}_2C_1 \times 3^{(2-1)}. \quad (3)$$

In similar manner, the number of combinations for '1 to 0' transition at 2 bit on Top I/O can be calculated as

$${}_2C_2 \times 3^{(2-2)}. \quad (4)$$

(3) Combination of events for charge recycling

Fig. 7 shows possible case of charge recycling on 2×2 bits stacked data bus.

Referring to Eq. (1) to (4), the number of combinations can be calculated for each event in Fig. 7. Summary is in Table II.

Table I Combination of 0 to 1 transition in 2 bits data bus

Case	#1	#2	
1	0 → 1	0 → 0	'0 to 1' transition at 1bit of 2bits ${}_2C_1 \times 3^{(2-1)}$
2	0 → 1	1 → 0	
3	0 → 1	1 → 1	
4	0 → 0	0 → 1	
5	1 → 0	0 → 1	
6	1 → 1	0 → 1	
7	0 → 1	0 → 1	$\rightarrow {}_2C_2 \times 3^{(2-2)}$

Therefore, a number of combination for charge recycling bits ($N_{CR_2 \times 2}$) can be calculated as follows;

$$\begin{aligned}
 N_{CR_2 \times 2} &= {}_2C_1 \times 3^{(2-1)} \times {}_2C_1 \times 3^{(2-1)} \times 1 \\
 &\quad + {}_2C_1 \times 3^{(2-1)} \times {}_2C_2 \times 3^{(2-2)} \times 1 \\
 &\quad + {}_2C_2 \times 3^{(2-2)} \times {}_2C_1 \times 3^{(2-1)} \times 1 \\
 &\quad + {}_2C_2 \times 3^{(2-2)} \times {}_2C_2 \times 3^{(2-2)} \times 2 \\
 &= \sum_{p=1}^2 \sum_{q=1}^2 {}_2C_p \times 3^{2-p} \times {}_2C_q \times 3^{2-q} \times \min(p, q)
 \end{aligned} \quad (5)$$

p and q are number of bits for '1 to 0' transient on Top and '0 to 1' transient on Bottom Driver respectively. This formula is derived from product of a number of recycled bits and a number of combination in Table II.

(4) Calculation of power reduction ratio

To calculate power reduction ratio by the charge recycling, power consumption of non-charge recycling case should be defined. It can be calculated by appearance probability of '0 to 1' transition on 4 bits. A number of combination for '0 to 1' transient bits in 4 bits data bus (N_{01_4}) can be calculated as;

$$N_{01_4} = \sum_{k=1}^4 {}_4C_k \times 3^{4-k} \times k \quad (6)$$

As for power reduction ratio on the 2×2 bits stacked data bus ($RR_{2 \times 2}$), it is derived from a ratio of $N_{CR_2 \times 2}$ and N_{01_4} from Eq. (5) and (6).

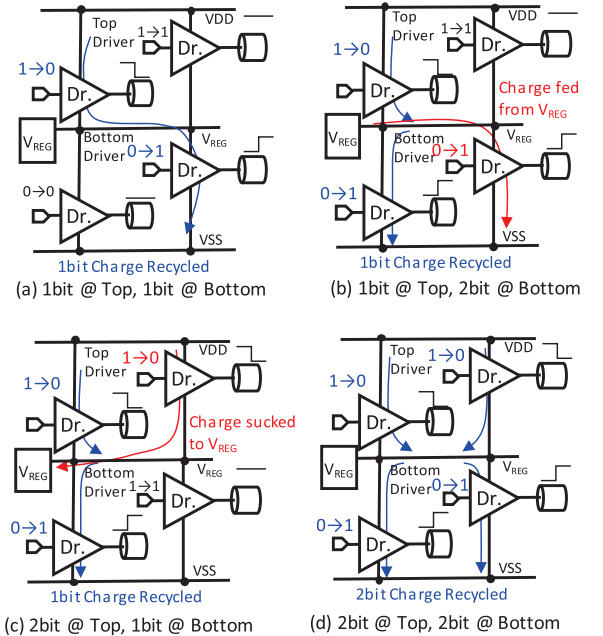


Fig. 7 Possible bits for charge recycling on 2×2 stacked bus

Table II Charge recycling in 2×2 bits data bus

Event	Fig.7	eq.	Recycled Bits	Number of Combinations referred to Chapter 3.2 (1)(2)
(a)	1	3	1 bit	${}_2C_1 \times 3^{(2-1)} \times {}_2C_1 \times 3^{(2-1)}$
(b)	1	4	1 bit	${}_2C_1 \times 3^{(2-1)} \times {}_2C_2 \times 3^{(2-2)}$
(c)	2	3	1 bit	${}_2C_2 \times 3^{(2-2)} \times {}_2C_1 \times 3^{(2-1)}$
(d)	2	4	2 bits	${}_2C_2 \times 3^{(2-2)} \times {}_2C_2 \times 3^{(2-2)}$

$$RR_{2 \times 2} = \frac{N_{CR_2 \times 2}}{N_{01_4}} = \frac{\sum_{p=1}^2 \sum_{q=1}^2 2C_p \times 3^{2-p} \times 2C_q \times 3^{2-q} \times \min(p, q)}{\sum_{k=1}^4 4C_k \times 3^{4-k} \times k} \quad (7)$$

3.3 Calculation formula for $N \times 2$ bits stacked data bus
As stated above, charge recycling can be possible between TSVs on Top and Bottom floors, and a number of combination for recycling bit in $N \times 2$ stacked bus can be obtained by extension of Eq. (5) and (6) to N bits.

$$N_{CR_N \times 2} = \sum_{p=1}^N \sum_{q=1}^N N C_p \times 3^{2-p} \times N C_q \times 3^{N-q} \times \min(p, q) \quad (8)$$

$$N_{01_2N} = \sum_{k=1}^{2N} 4C_k \times 3^{2N-k} \times k \quad (9)$$

(1) Positive and negative factor consideration

As described above, capacitance is positive factor for increasing the recycling bit. In contrast, wider bit width (N) needs longer wiring of V_{REG} node, and it causes timing offset between charge injection and subtraction on V_{REG} node. The timing offset is negative factor, equivalently decreasing the recycling bit. The positive and negative factor on $N \times 2$ bits bus are described as a_N and b_N respectively, then Eq. (8) can be expressed as follows.

If \geq , then

$$N_{CR_N \times 2} = \sum_{p=1}^N \sum_{q=1}^N N C_p \times 3^{N-p} \times N C_q \times 3^{N-q} \times (\min(p, q) - b_N)$$

If $< q$, then

$$N_{CR_N \times 2} = \sum_{p=1}^N \sum_{q=1}^N N C_p \times 3^{N-p} \times N C_q \times 3^{N-q} \times (\min(p, q) + a_N - b_N) \quad (10)$$

If p is greater than q , the positive factor does not work to increase N_{CR} because theoretical maximum number of recycle bit is q .

(2) Positive and negative factor extension

Positive and negative factors (a_N, b_N) become more significant as the bus width (N) increases. When multipliers for doubling data bus width at a_N and b_N are set to m_p and m_n respectively, Eq. (10) can be expressed as shown in Fig. 8.

$N \times 2bit$	$N_{CR_N \times 2} = N_{CR_N} + a_N - b_N$
$N \times 2bit$ Bus	
↓ X2 width	positive : m_p times, negative : m_n times
$N \times 2bit$ $N \times 2bit$	
$2N \times 2bit$ Bus	$N_{CR_2N \times 2} = N_{CR_2N} + a_N m_p - b_N m_n$
↓ X2 width	positive : m_p times, negative : m_n times
$N \times 2bit$ $N \times 2bit$ $N \times 2bit$ $N \times 2bit$	
$4N \times 2bit$ Bus	$N_{CR_4N \times 2} = N_{CR_4N} + a_N m_p^2 - b_N m_n^2$

Fig. 8 Number of combination for recycling bit with doubling bus width

These parameters will be derived through simulation results in later chapter. The power reduction ratio of $N \times 2$ bits ($RR_{N \times 2}$) can be obtained by Eq. (9) and Eq. (10).

$$RR_{N \times 2} = \frac{N_{CR_N \times 2}}{N_{01_2N}} \quad (11)$$

4. Clock management and data reception

4.1 Clock transmission

The pair of clocks is fed to receiver side using stacked I/O configuration to expect frequent charge recycling. Fig. 9 depicts clock waveforms of Top and Bottom drivers. As shown in this figure, clocks have $0.5V_{DD}$ voltage swing likely to data transmission. The clocks are complementary and equalized on V_{REG} node ($0.5V_{DD}$) in every clock period.

4.2 Receiver

Fig. 10 illustrates block diagram of Receiver for 1×2 bit bus. The Receiver has level shifter and two comparators.

The transmitted clocks (ClkU, ClkD) are buffered by level shifter in Receiver, and the level shifter generates local clocks (Clk, ClkB) of full voltage swing (V_{DD}).

Fig. 11 depicts circuit schematic and incoming clock signal for level shifter.

As shown in the figure, the level shifter can be configured with a small number of transistors and acts as a digital behavior (ON and OFF).

5. Simulation results

Each TSV is modeled by referencing [27, 28, 29, 30]. In this assumption, TSV length, TSV diameter and oxide thickness

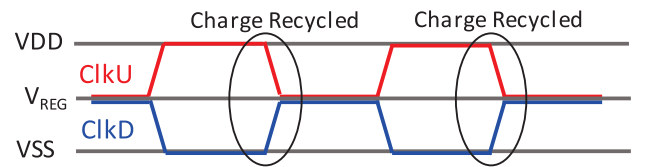


Fig. 9 Clock signal transmission

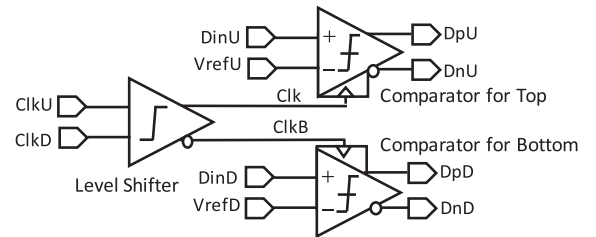


Fig. 10 Block diagram of receiver (1×2 bit)

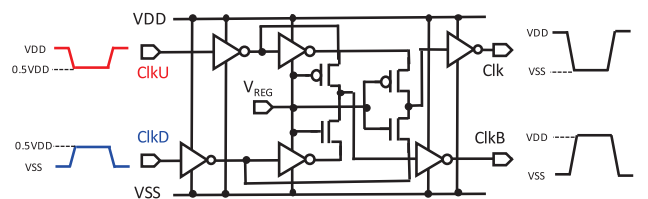


Fig. 11 Level shifter and local clock generation

are 100 μm , 50 μm and 0.5 μm respectively. An effective capacitance of the TSV is about 0.84 pF, which would be equivalent to 5 mm metal wire in [26].

5.1 Power reduction ratio in data transmission

Fig. 12 shows a breakdown of power consumption for $N \times 2$ bit data bus with and without charge recycling.

To calculate power reduction ratio corresponding to Eq. (11), power consumptions of Data Driver and LVS are took into account in Fig. 12. Fig. 13 shows power reduction ratio of calculation by Eq. (11) and the simulation results.

In the calculation, parameters of a_N , b_N , m_p and m_n are set as Table III for the best fitting to the simulation results. As shown in Fig. 13 and Table III, results of calculation and simulation are well matched using reasonable values of a_N , b_N , m_p and m_n . Hence, the Eq. (11) is useful to estimate power reduction ratio of the charge recycling with given N in this process technology.

5.2 Power efficiency

Power efficiency of parallel data bus is defined as power consumption (Jules) per channel bandwidth (bit per second) for single bit data transmission (bit). Fig. 14 shows power efficiencies of proposed scheme (This Work).

In this power efficiency calculation, power dissipation for

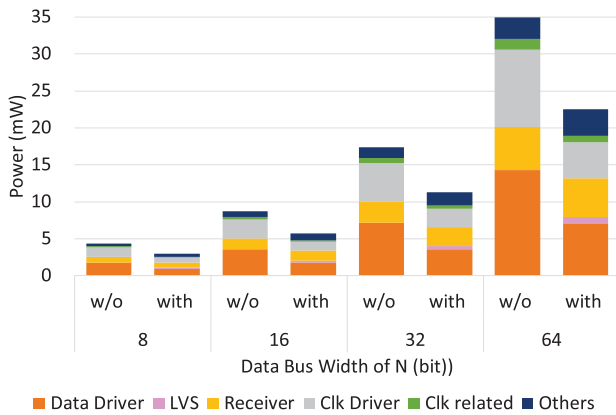


Fig. 12 Power comparison between w/o and with charge recycling

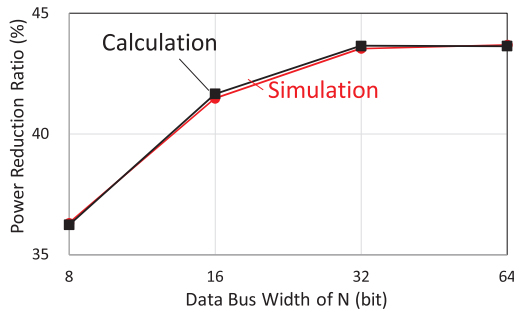


Fig. 13 Driver power comparison

Table III Calculation parameters

a_g	1.1
b_g	0.25
m_p	2.3
m_n	2.45

all blocks are considered. As shown in the figure, the power efficiency is improved as bus width becomes wider, but degree of improvement decreases as bus width increases. N should be set to 32 or 64. This figure depicts power efficiencies with (solid line) and without clock (dotted line).

In this simulation, one clock line is allocated to 8 bit data bus for data acquisition. Performances for Reference [20, 25] and this work are summarized in Table IV.

In [25], clock is assumed to have full V_{DD} swing. In a comparison to [25], the power efficiency is 15% worse in data transmission. This comes from power dissipation on LVS for capacitance reduction. However, considering clock transmission, the power efficiency becomes comparable to [25] thanks to charge recycling and local level shifter on clock line. Ref. [20] has very small size than others and it comes from i) simple CMOS driver (no charge recycling), ii) low TSV capacitance (200 fF) and iii) no voltage regulator for excessive low V_{DD} (0.14 V). Therefore, the size can not simply be compared to others.

6. Conclusion

The formula to calculate power reduction ratio is derived from transition probability for pure random data stream. The reduction ratio is for the proposed charge recycling scheme to normal scheme (non-charge recycling). The formula has good correlation with simulation result of driver's power dissipation, and it gives easy method to perceive the power reduction effect using charge recycling for early stage of system design in 3D chip integration.

The proposed data and clock transmission scheme has a

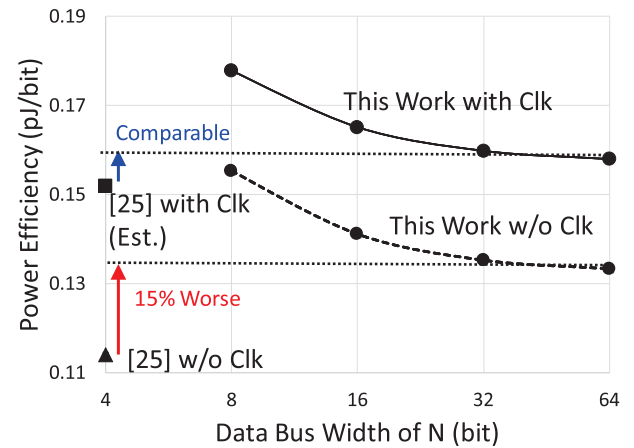


Fig. 14 Power efficiency comparison

Table IV Performance summary

	Ref. [20]	Ref. [25]	This Work
Driver V_{DD} (V)	0.14	0.9	1.0
Process Technology	Standard 45nm	40nm with Trench Cap.	Standard 65nm
Charge Recycling	No	Yes	Yes
Size of Tx & Rx for 2bit bus (μm^2)	336	1608.5	703.46
Power Efficiency w/o Clk Trans. (pJ/bit)	0.13	0.114	0.135
Power Efficiency with Clk Trans. (pJ/bit)	0.173 (Estimation)	0.152 (Estimation)	0.160

potential to be comparable power efficient (0.16 pJ/bit) with prior work (0.152 pJ/bit) of more advanced and expensive technology [25]. The power efficiency can be achieved by wide bit bus ($> 32 \times 2$ bits) and charge recycling for data and clock transmission. The size of proposed Tx and Rx macro has 56% smaller size to the prior work thanks to Local Voltage Stabilizer (LVS) and simple comparator with compact level shifter. The proposed scheme suggests one promising candidate for the data transmission methodology in 3D chip integration through TSVs.

Acknowledgments

This work was supported by JSPS KAKENHI Grant Number JP17K00090. This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., Mentor Graphics, Inc. and Renesas Electronics Corporation.

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