

Design of self-referenced wide input voltage range LDO using enhanced current mirror buffer and improved lead compensation

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Abstract This letter presents the self-referenced architecture to simplify design process and current mirror based power stage with wide input voltage to expand the application range of low-dropout (LDO) regulator. Featuring a BiCMOS symmetrical operational transconductance amplifier (OTA) whose input and power supply are also the output of LDO, the LDO itself is a voltage reference as well as a voltage regulator. Improved phase lead compensation is applied with much smaller compensation capacitor, and enhanced current mirror (ECM) buffer is introduced. Experimental results of the proposed LDO in a 0.18 μ m BCD process verified this self-referenced structure. The measured maximum input voltage is 12 V and the power supply rejection (PSR) is -40 dB at 50 KHz. The line regulation is 0.34 mV/V and total quiescent current is about 8.2 μ A at light load.

Keywords: LDO, mixed-mode bandgap technique, self-referenced, wide input, lead compensation

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The input voltage of LDO is usually near its output voltage otherwise the power efficiency will be poor. But sometimes a wide input range is needed. For example, a linear regulator with wide input voltage can be used as a pre-regulator for the internal analog and digital supply for a switching mode power supply (SMPS). Although fully on-chip design is today's research focus of LDO [1, 2, 3, 4, 5], for a wide input voltage range LDO or a separate LDO chip which is not integrated together with its load in a SoC, it is still usually designed to have an off-chip capacitor [6, 7, 8, 9, 10].

A typical LDO regulator, whether a fully integrated one or with external capacitor, comprises the power transistor, an error amplifier (EA), compensation network, feedback circuit and a voltage reference generator, as shown in Fig. 1(a). Although it is easier to design a LDO with PMOS as the power transistor, NMOS is also an alternative [11, 12]. Flipped voltage follower (FVF) has smaller output impedance and many LDOs have been designed based on it [1, 4, 13, 14]. Various methods, such as pole-zero cancellation [15], nested miller compensation (NMC) [5], damping-factor-control [16], Q-reduction [17], buffer impedance attenuation (BIA) [18] and pole-zero tracking [19], have been proposed for frequency compensation of LDO. Corresponding methods for optimization of load

DOI: 10.1587/elex.17.20200120 Received March 30, 2020 Accepted May 7, 2020 Publicized May 20, 2020 Copyedited June 10, 2020 transient response and PSR are also included in these works. Digital or digitally assisted LDO [2, 3, 20] has also been proposed to improve regulation and transient response.



Fig. 1 (a) Conventional architecture of LDO (with or without external capacitor). (b) New self-referenced architecture of LDO

Although various structures and advanced techniques have been proposed to improve LDO's performance, they are still based on the basic architecture. In addition, voltage reference and voltage regulator are usually designed separately. Some of LDOs don't even have the voltage reference integrated together. Furthermore, LDOs with wide input voltage are seldom reported. With a wide input voltage, the application range of LDO can be extended, not only for battery powered portable application, but also for automotive and industrial applications.

We present a novel architecture of LDO as shown in Fig. 1(b). In this structure, the feedback network, voltage reference generator and the EA have been merged into a single self-referenced EA, whose power supply is V_{out} instead of V_{in} . Both the input and power supply of the EA are directly connected with the output node of the LDO, making the LDO itself a voltage reference as well as a voltage regulator. Based on this simpler architecture, potential advantages such as smaller chip size, lower power consumption and lower line regulation can be expected. In this letter, we use this self-referenced architecture to design a wide input range LDO. A new enhanced current mirror (ECM) buffer is

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introduced into the power stage. Applying phase lead compensation to this new architecture, the needed compensation capacitor can be reduced to one eighth of the original value.

2. Self-referenced LDO with wide input voltage range

Fig. 2 shows the structure of the proposed self-referenced LDO. The four transistors, each inside a circle, are laterally double-diffused MOSFET (LDMOS), with high blocking voltage BVDSS = 12 V. The rest of transistors used in this design are all regular MOSFETs.



Fig. 2 Structure of the proposed self-referenced wide input LDO

Power transistor M_{P2} is driven by a diode-connected transistor M_{P1} , thus forming an ordinary current mirror (OCM). M_{N1} is a source follower which isolates the low voltage control circuit from the possible high input voltage. Using this OCM buffer, the original low frequency gate pole p_{gate} of the power transistor has now been pushed to a much higher frequency. In addition to this OCM buffer [21], another two current mirrors are added. As a result, we only need to control a much smaller device M_{N3} to regulate V_{out} . The current density I_{DS}/W of the transistors in the ECM buffer is a constant, so the voltage gain from gate voltage of M_{N3} to gate voltage of M_{N4} is 1. The total DC voltage gain of ECM buffer plus power stage from input control voltage V_{ctrl} to V_{out} is

$$\frac{V_{out}}{V_{ctrl}} = g_{mN4} \times 20 \times R_L \tag{1}$$

where g_{mN4} is the transconductance of M_{N4} and R_L is the equivalent load resistance.

In addition to the output pole, the second important pole in the ECM buffer and power stage is the mirror pole p_{gate} at the gate of M_{P2}. From calculation and simulation, when R_L varies over three orders of magnitude, the DC gain, mirror pole p_{gate} and output pole p_{out} are as shown in Table I.

In Table I, C_P is the parasitic capacitance at power transistor's gate node, which is 11 pF; C_L is the output capacitance,

Table I	Gain and	poles of	f buffer	plus	power	stage
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	gain/dB	pout/Hz	p_{gate}/Hz
Expression	$20g_{mN4}R_L$	$\frac{1}{2\pi R_L C_L}$	$\frac{g_{mP1}}{2\pi C_P}$
$R_L = 100$	23	723	115M
$R_L = 100 \text{K}$	35	0.7	676K

which is 2.2 μ F. When R_L changes from 100 Ω to 100 K Ω , g_{mN4} changes from 7.7 mS to 31 μ S. p_{gate} is far beyond the gain-bandwidth product (GBW) and power stage plus ECM buffer can be viewed as a single pole system.

The control voltage V_{ctrl} is generated by the selfreferenced OTA which will be discussed in the next Section. But before this control loop operates normally, the output voltage must be above a certain value. This part of job is done by the start-up circuit.

Two output voltage detectors (OVD) are adopted to monitor the value of V_{out} during start-up process. They work on a similar principle as in [22]. When V_{out} ramps to its final value, OVD2 responds to replace OVD1. OVD2 consumes a current of 0.5 μ A from V_{out} . The start-up circuit consumes a current of about 0.5 μ A from V_{in} . Besides, it should be noticed that because of the existence of the OCM formed by M_{P1} and M_{P2}, there will always be a current equaling 1/20 of load current which flows directly from V_{in} to ground, resulting a current efficiency smaller than 95%.

3. Implementation of self-referenced OTA

The self-referenced OTA outputs an analog signal V_{ctrl} to complete the feedback loop. This unique OTA is shown in Fig. 3. The feedback network, voltage reference generator and the EA have been merged in this self-referenced OTA. In Fig. 3, part (a) is a conceptual schematic of this self-referenced OTA, in which there is a symmetrical OTA working essentially as a current mirror. The transistor level schematic of this symmetrical OTA is as shown in part (b).

3.1 Principle of the built-in voltage reference generator Here we define current density J_Q of a bipolar transistor with N units as the current flowing through a single unit. For example, if the collector current of a bipolar transistor Q_1 with N parallel units is I_{C1} , its current density is

$$J_{Q1} = \frac{I_{C1}}{N} \tag{2}$$

If two bipolar transistors operate at unequal current densities, the difference between their base-emitter voltages ΔV_{BE} is proportional to the absolute temperature (PTAT) [23]. In Fig. 3, to generate such a PTAT ΔV_{BE} , current mirrors composed by bipolar transistors are used, which is a big difference from Brokaw's [24] or Banba's [25] voltage reference. Suppose the current mirror is ideal, the relationship of Q_{N3} and Q_{N4}'s current densities will be

$$\frac{J_{Q3}}{J_{Q4}} = \frac{8/1}{3/3} = \frac{8}{1} \tag{3}$$

The voltage difference $V_{BE3} - V_{BE4}$ between their baseemitter voltages, which is also the difference between baseemitter voltages of Q_{N1} and Q_{N2} as well as the voltage across



Fig. 3 (a) Conceptual schematic of the self-referenced OTA. (b) Transistor level schematic of the symmetrical OTA used in (a)

 R_{N2} , then equals $V_T \ln 8$. Thus, the current flowing through R_2 is a PTAT one:

$$I_{R2} = \frac{V_T \ln 8}{R_2}$$
(4)

According to the ratios of current mirrors and the BJT's corresponding number of units, the relationship of Q_{N1} 's collector current and Q_{N2} 's collector current is

$$I_{C1} = 3J_{Q1} = 3J_{Q3} = 3 \times (J_{Q4} \times 8) = 3 \times (J_{Q2} \times 8) = 3I_{C2}$$
(5)

Since R_3 is in parallel with Q_{N1} , its current is complementary to the absolute temperature (CTAT):

$$I_{R3} = \frac{V_{BE1}}{R_3}$$
(6)

Combining Eq. (4), Eq. (5) and Eq. (6), V_{out} is derived as

$$V_{out} = V_{BE1} + (I_{R3} + I_{C1} + I_{R2})R_1$$

$$\approx V_{BE1} + (I_{R3} + I_{C1} + I_{C2})R_1$$

$$= V_{BE1}(1 + \frac{R_1}{R_3}) + 4 \times V_T \ln 8 \times \frac{R_1}{R_2}$$
(7)

where R_1 , R_2 and R_3 can be used to adjust the target output voltage like the feedback resistors in Fig. 1(a). At the same time, the generated V_{out} is PVT insensitive. The output structures of Brokaw's [24] and Banba's [25] bandgap voltage references can be called voltage-mode and current-mode [26] respectively, whereas it is a mixed-mode in this voltage reference generator.

3.2 Symmetrical OTA and frequency compensation

The BiCMOS symmetrical OTA in Fig. 3(b) uses a pseudodifferential input stage [27], Q_{N3} and Q_{N4} , which also forms a current mirror with Q_{N1} and Q_{N2} respectively. The number of units and current ratio are decided by the target V_{out} and the consideration on base current compensation. When V_{out} increases, both V_{BE1} and V_{BE2} increase subsequently, whereas the former has a larger increase, which eventually makes V_{ctrl} decrease. With $R_2 = 60 \text{ K}\Omega$, $R_1 = 592 \text{ K}\Omega$ and $R_3 = 230 \text{ K}\Omega$, the power consumption of this OTA @ V_{out} = 4 V is as shown in Table II at room temperature. The total power consumption of this self-referenced OTA is calculated to be less than 7.2 μ A.

Table II Power consumption of the symmetrical OTA @ $V_{out} = 4 \text{ V}$

I_{R1}	Bias	I_{Q3}	I_{Q4}	I _{MN3}	I_{MN4}
5.5 µA	0.17 µA	0.69 µA	0.26 µA	0.26 µA	0.26 µA

With an external capacitor C_L of 2.2 μ F, the output pole p_{out} is very small and is the dominant pole. With a load capacitance of about 20 fF including both its internal parasitic capacitance and the input capacitance of the ECM buffer, the output pole of this OTA p_{EA} is about 30 KHz.

Adding a capacitor C_c across the upper member of the feedback divider will introduce a left-half-plane (LHP) zero and achieve phase lead compensation. As shown in Fig. 4, if R_{f2}/R_{f1} is smaller, the effect of phase lead compensation will be more noteworthy.



Fig. 4 Principle of phase lead compensation

In this work, we use the basic principle of phase lead compensation in Fig. 4, but add the capacitor C_c to an internal node of this OTA as shown in Fig. 3 instead of adding it across R₁. Fig. 5 is the small signal circuit of this self-referenced OTA. The transfer function from V_{out} to V_{BE1} can be simplified as $\frac{1/g_{Q1}}{1/g_{Q1}+R_1}$. R_1 and $1/g_{Q1}$ form the equivalent divider network of this self-referenced OTA, whose functions correspond to R_{f1} and R_{f2} in Fig. 1 respectively.

Applying nodal voltage analysis method to Node ① and Node ② in Fig. 5,

$$\begin{cases} \frac{V_{GS_N3} - V_{out}}{1/sC_c} - g_{Q4}V_{BE1} + \frac{V_{GS_N3}}{1/g_{mN3}} = 0\\ V_{GS_N3}g_{mN3} - g_{Q4}V_{BE2} + \frac{V_{ctrl}}{R_{out_EA}} + \frac{V_{ctrl}}{1/sC_{out_EA}} = 0 \end{cases}$$
(8)

Solving Eq. (8), it is derived that

3



Fig. 5 Small signal circuit of this self-referenced OTA

$$\begin{cases} V_{GS_N3}(s) = \frac{g_{Q4}V_{BE1} + sC_cV_{out}}{g_{mN3} + sC_c} \\ R_{out_EA}(g_{m_N3}g_{Q4}V_{BE1} - g_{m_N3}g_{Q4}V_{BE2} \\ V_{ctrl}(s) = -\frac{+g_{m_N3}sC_cV_{out} - g_{Q4}sC_cV_{BE2})}{(g_{m_N3} + sC_c)(1 + sR_{out_EA}C_{out_EA})} \end{cases}$$
(9)

Thus, the introduced LHP zero can be approximated as

$$p_z = \frac{1}{2\pi} \frac{g_{Q4} V_{BE1}}{C_c V_{out}} \approx \frac{1}{2\pi} \frac{g_{Q4}}{C_c} \frac{1/g_{Q1}}{R_1} = \frac{1}{2\pi} \frac{1}{R_1 C_c} \frac{g_{Q4}}{g_{Q1}}$$
(10)

Comparing this result with Fig. 4, the obtained LHP zero is further reduced by a factor of g_{Q4}/g_{Q1} , which means we only need a much smaller C_c to achieve the same effect of phase lead compensation. In this work, $g_{Q4}/g_{Q1} \approx 1/8$. To cancel the output pole of this OTA which is about 30 KHz, the needed C_c is about 0.5 pF. Otherwise, a compensation capacitor of 4 pF is needed.

Fig. 6 is the simulated Bode plot of the LDO and the output pole of LDO (see Table I) is the dominant pole. At heavy load, with C_c to cancel the output pole of EA, the phase margin (PM) increases from almost 0 to 60°, and the GBW at $R_L = 100 \Omega$ is about 0.3 MHz. At light load, the DC gain increases from 53 dB to 66 dB, whereas the GBW decreases to about 1.2 KHz and the PM is 90°. Good stability of the LDO with improved phase lead compensation is achieved



Fig. 6 Bode plot of the LDO under different load conditions

over the total load range.

4. Experimental results

The proposed self-referenced LDO has been fabricated with a 0.18 μ m BCD process. The blocking voltage *BVDSS* of the used LDMOS is 12 V. Fig. 7 is the microphotograph of this LDO. The chip area is 0.68 mm × 0.27 mm. The five main parts—power stage plus ECM buffer, self-referenced OTA, OVD1, OVD2, start-up circuit—are marked with rectangles and it is noticed that the latter three ones cover almost half of the total area. By using resistors and capacitors with higher density, the chip area can be reduced.



Fig. 7 Microphotograph of the self-referenced LDO

Fig. 8 shows the testing setup of this LDO. C_L is a MLCC capacitor of 2.2 μ F. A p-type power MOSFET S_P of IRF4905 is used as a switch to change load state. An AC source is coupled through C_{cp1} and C_{cp2} for measuring line transient response and power supply rejection.



Fig. 8 Testing setup of this LDO

Fig. 9 shows the measured line transient response. The DC value of input voltage is 5 V. When the load current I_L is 50 mA and the peak-to-peak noise of V_{in} is 200 mV, the measured peak-to-peak ripple at the output is about 2 mV, which translates into a PSR of -40 dB at 50 KHz.

Fig. 10 shows the measured load transient response. The



Fig. 9 Measured line transient response at $I_L = 50 \text{ mA}$



Fig. 10 Load transient: pulse signal to change load state and Vout

pulse signal turns on or off S_P and R_L is fixed to be 100 Ω , which simulates a load step 0–40 mA. When pulse signal turns high, it equals load current changing from 40 mA to 0 mA and vice versa. As Fig. 10(a) shows, the output voltage remains at about 4 V with load changing abruptly.

Fig. 11 shows the measured line regulation. With V_{in} varying from 5 to 12 V, a 2.4 mV voltage change of V_{out} is observed, which translates into a line regulation of 0.34 mV/V.



Fig. 11 Measured line regulation at $I_L = 40 \text{ mA}$

Fig. 12 shows the measured temperature characteristics of the proposed LDO without trimming for three samples. Each graph is like a down facing parabola which demonstrates the temperature behavior of a first-order bangdap reference. This verifies the feature of this LDO being a voltage reference as well.



Fig. 12 Measured temperature characteristics of three untrimmed samples at $V_{in} = 5$ V and $I_L = 40$ mA

Table III is the performance summary of this selfreferenced LDO and comparison with other state-of-the-art works. Due to the adopted new self-referenced architecture, this design prototype features higher integration level. The originally separate parts—feedback dividers, voltage refer-

 Table III
 Performance summary and comparison with other works

	Tech.	Area	<i>IQ</i> *	C_L	Max. IL	Line regu.
	(nm)	(mm ²)	(µA)	(μF)	(mA)	(mV/V)
[8]	600	0.3	8	1	30	N/A
[10]	N/A	N/A	2	2.2	200	2
[28]	180	0.024^{\dagger}	135	1	100	22.7
[29]	90	0.0027^{\dagger}	9.3	1	50	14
[30]	350	0.226	4	1-10	100	17
[21]	180	0.039 [†]	0.9	0.47	50	7.25
[31]	180	0.216	5.2	1	150	6.75
This	180	0.184	8.2	2.2	50	0.34
*at lig	nt load				•	

it light load

[†]not integrating the voltage reference inside

ence, and voltage regulator—are integrated together naturally. Compared with [8] which is also a wide input LDO, this work utilizes current mirror based power stage, which greatly reduces the number of used DMOS transistors, and all the control circuits can be designed in the low output voltage domain. Furthermore, thanks to this self-referenced architecture, this work features low line regulation, which is only 0.34 mV/V.

5. Conclusion

A new self-referenced architecture of LDO has been presented, which makes the LDO itself a voltage reference as well as a voltage regulator. This new topology makes feedback-divider resistors unnecessary and enhanced phase lead compensation can be applied. Both the input and power supply of this OTA are directly connected with the output of the LDO. This new architecture has been applied to a LDO with wide input voltage. Using current mirror based power stage, only four LDMOS transistors are needed, and all the control circuits can be designed in the low output voltage domain. A two-stage start-up circuit is designed. Measurement results have verified the feasibility of this new architecture. High integration level (reference and regulator are integrated together naturally) and low line regulation have been achieved. This self-referenced architecture can be applied to LDOs with or without external capacitors and more improvements may be obtained.

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