

Research on the influences of well structure on dose rate effects in 65nm CMOS circuit

Qian CHEN^{1, 2}, Jianwei HAN^{1, 2}, Yingqi MA^{1, 2, a)}, Sai LI^{1, 2}, Jingtian LIU³, Yaqing CHI³, and Bin LIANG³

Abstract A short-time high-dose gamma ray will produce many electronhole pairs by the Compton effects in various semiconductor materials. Then pulse current will be generated in the devices and electronic system and affect their normal operation, which is called the Dose Rate Effects (DREs). Based on three-dimensional (3D) technology computer aided design (TCAD) simulations, the impacts of well structures on the DREs in 65-nm bulk CMOS inverter which is the most basic circuit unit are investigated. In this paper, the extend Gamma Radiation Model is used in simulations for effectively simulating the generation of electron-hole pairs in circuits. And present a idea for radiation hardening of bulk silicon CMOS circuits approach to DREs through optimization of well structure. The results of the simulations show that deep P-well (DPW) structure effectively reduces pulse amplitude of the voltage while the deep N-well (DNW) structure reduces the pulse amplitude only in high doping concentration. In addition, the pulse amplitude decreases with the doping concentration of deep well increasing. The mechanism is analyzed from the aspects of charge collection and potential change.

Keywords: well structures, CMOS, dose rate effects, bipolar amplification effect

Classification: Electron devices, circuits and modules (silicon, compound semiconductor, organic and novel materials)

1. Introduction

The engineer of Bell Labs, ROGER SC, observed the radiation response of a diode in a gamma radiation environment for the first time in a ground test [1]. He and WIRTH JL jointly proposed that gamma rays produce photocurrent in semiconductor devices through ionization, which affects the normal operation of the device [2]. A short-time high-dose gamma ray affects the operation of semiconductor devices through ionization, which is called the Dose Rate Effects (DREs). References [3, 4] analyze the DREs of semiconductor PN junctions and four-layer semiconductor structures. Researcher D.C. Sullivan analyzed and studied the DREs of the MOS transistor [5]. P.K. Skorobogatov and A.Y. Nikiforov et al. studied the equivalence of laser simulated dose rate effect and developed the laser test of dose rate effects [6, 7]. Some researchers focus on the unique latch window phenomenon of transient dose rate effects and con-

DOI: 10.1587/elex.17.20200205 Received June 8, 2020 Accepted June 26, 2020 Publicized July 9, 2020 Copyedited July 25, 2020 duct related research [8, 9, 10, 11, 12, 13, 14, 15]. Guillermo Vera and Marios Pattichis of the University of New Mexico and Daniel Llamocca of the University of Oakland and others conducted an experimental study on the instantaneous dose rate flipping effect of SRAM-type FPGAs in the 90nm process [16]. It found the threshold was 3×10^8 rad (Si)/s. Researchers at Tsinghua University conducted an experimental analysis of the microcontroller's dose rate disturbance effect [17]. Korean researchers conducted experimental and simulation studies on several CMOS circuits and linear circuits [18]. The disturbances, flips and latch-up phenomena of the device under instantaneous radiation environment are analyzed. The research of DREs on CMOS circuits has gradually attracted the attention of researchers from various countries in recent year.

Bulk CMOS technologies are widely used in integrated circuits and electronic system. The dual-well (DW) and triple-well are basic well technology in CMOS technology. The triple-well (TW) structures divides into deep P-well (DPW) and deep N-well (DNW). The researches of the well structure influence on the radiation effects mainly focus on the single event effects (SEEs). Such as the P+ deep well has little effect on the I-V characteristics of the device, but it can effectively mitigate the influence of the substrate on the well potential [19]. Studies show that heavily doped deep P+ well can improve single event upset (SEU) threshold for SRAM [20]. The deep N+ well can change the vertical electric field and affects the charge collection [21]. References [22] found the N+ deep well has a significant effect on the SEU rate in the SRAM. Reference [23] suggest that selectively implanted deep N-well is an efficient method to reduce the single event transients (SETs) pulse width and cross-section, and thus mitigates the soft error rate induced by SETs. Reference [24] shows the N+ deep well results in an increase on multiple bit upsets (MBU) in the SRAM under the irradiation test. These studies all point out the well structure has a certain modulation effect in SETs and SEU.

The DREs differs with SEEs in that many electron-hole pairs produced by ionization caused by the Compton effects, forming a globally uniform current in the circuit because of the high photon energy and strong penetrability of gamma rays. Therefore, the well structure plays a more important role to form photocurrent in DREs than in SEEs, and the impacts of well structures on the DREs in CMOS circuits are worthy to research. However, none of these studies has focused on this point. It is well known the inverter is the basic unit of the CMOS circuit. In this paper, the 65nm CMOS inverter is selected as the research object, and the

¹ National Space Science Center, Chinese Academy of Sciences, Beijing, 100190, China

² University of Chinese Academy of Sciences, Beijing 100049, China

³ National University of Defense Technology, Changsha 410073, China

^{a)} myq@nssc.ac.cn

effects of the well structure on the DREs of the CMOS circuit is studied using the 3D TCAD simulations. And further explored the effect of deep well doping concentration. A method of DREs radiation-hardening technique for bulk CMOS circuits through optimization of well structure is proposed based on simulation results and the analysis of its physical mechanism.

2. Simulation setup

The simulations performed in 65-nm bulk CMOS inverter using Sentaurus TCAD. All simulations conducted using the YINHE computing cluster in the National University of Defense Technology in China. The 3D TCAD models are calibrated to meet with electrical characteristics got from a 65-nm commercial Process Design Kit (PDK). The 3D TCAD devices structures are shown in Figure 1. Doping parameters are shown in Table I. For the CMOS inverter, the PMOS transistor size is W/L = 210nm/200nm and the NMOS transistor size is W/L = 210nm/200nm. The dose rate of the Gamma irradiation is 1×10^{11} rad (Si)/s in simulations.

The impacts of different types of deep well doping concentrations on the DREs of inverters were investigated. We only change the doping concentration of the deep well and keep others the same, comparing doping concentration with



Fig. 1 3D TCAD devices structures. (a) DW structure device; (b) DNW structure device; (c) DPW structure device.

Table I Doping parameters of the inverters.

Doping Target	Doping Concentration
P Well	8×10 ¹⁷ /cm ³
N Well	1×10 ¹⁷ /cm ³
P Substrate	1×10^{16} /cm ³
N+ Deep Well	1×10^{18} /cm ³
P+ Deep Well	1×10 ¹⁸ /cm ³

 2×10^{17} /cm3, 1×10^{18} /cm3 and 5×10^{18} /cm3 in DPW and DNW structures.

The following physical models were used: (1) Fermi-Dirac statistics, (2) band-gap narrowing effect, (3) doping dependent SRH recombination and Auger recombination, (4) temperature, doping, electric field and carrier-carrierscattering impact on mobility, (5) The extended Gamma Radiation Model. Unless otherwise specified. The default models and parameters provided by Sentaurus TCAD N-2017.09-SP1 were used.

The Gamma Radiation Model provided by Sentaurus TCAD is used to simulate the total ionizing dose (TID) effects. For the TID effects, the generation of the electronhole pairs due to radiation is an electric field-dependent process [25] and modeled as follows:

$$\mathbf{G} = g_0 \times \mathbf{D} \times \mathbf{Y}(F) \tag{1}$$

$$Y(F) = \left(\frac{F + E_0}{F + E_1}\right)^m \tag{2}$$

Where D is the dose rate of the Gamma irradiation, g_0 is the carrier generation rate of the silicon dioxide material. F is the electric field and E_0 , E_1 , and m are constants.

To effectively simulate the DREs of CMOS inverter, the extended Gamma Radiation Model is used in simulation. The TID model includes charge generation and collection, so there will be electric field effects. The DREs model only contains the charge generation process and is not affected by the electric field effect, and the collection process is included in the physical model (4) mentioned above. For the DREs, the generation of the electron-hole pairs due to radiation is directly proportional to the dose rate of the Gamma irradiation with a proportionality factor [26, 27] and modeled as follows:

$$G = g_1 \times D \tag{3}$$

Where D is the dose rate of the Gamma irradiation, g_1 is the carrier generation rate of the silicon material. This extended model is clearly applied in Reference [28], and its simulation results are in good agreement with experimental confirmation.

In the simulation, we converted the depth distribution of gamma rays to distribute the generated electron-hole pairs in the device, as is the case with traditional SEE. Due to the strong penetration of gamma rays and the small size of semiconductor devices, we estimate the electron-hole pairs are generated uniformly in the material, so the electronhole pairs are evenly distributed. In the conventional SEE setting, the electron-hole pairs are continuously attenuated on the incident track and Gaussian on the lateral diffusion. In short, the location and distribution of generated electronhole pairs are different.

3. Results

Figure 2 provide the responses of voltage in different well structures inverters after irradiation. No effect of low input and high input on the trend of the pulse amplitude of voltage in different well structure was demonstrated in the simulation results. Significantly decreasing amplitude was observed in DPW compared with DNW and DW. Therefore, we chose to take the input high as an example to further explore the influence of well doping concentration and its physical mechanism.

The voltage responses of different doping concentration of the deep well in both DNW and DPW structures inverters after irradiation are illustrated in Figure 3. A similar trend was observed in both DNW and DPW structures. As the doping concentration of the deep well increases, the pulse amplitude decreases. DPW showed better effects on the voltage pulse amplitude compared with DNW in same doping concentration.



Fig. 2 The outputs of different well structure inverters after radiation. (a) Input is low; (b) input is high.



Fig. 3 The outputs of inverters under radiation with doping concentration changing. (a) DNW structure device; (b) DPW structure device.

Туре	Concentration	Pulse Amplitude	Comparison With DW
DW	NONE	88mV	0
DNW	2×10 ¹⁷ /cm ³	100mV	+13%
DNW	1×10 ¹⁸ /cm ³	80mV	-9%
DNW	5×10 ¹⁸ /cm ³	50mV	-43%
DPW	2×10 ¹⁷ /cm ³	64mV	-27%
DPW	1×10 ¹⁸ /cm ³	50mV	-43%
DPW	5×10 ¹⁸ /cm ³	25mV	-72%

Table II Pulse amplitude of TW compared with DW under radiation.

The simulation results of different doping concentration deep well in DNW and DPW inverters are compared with the DW structure in Table II. It is found the pulse amplitude of voltage in DPW structure was significantly decreased comparing with the DW structure. The pulse amplitude in DNW structure is smaller than the DW structure only at higher doping concentration. The results show that compared with DW, DPW can effectively reduce the amplitude, and DNW can reduce the amplitude under certain conditions. As doping increases, the ability to reduce amplitude increases in both DNW and DPW. The mechanism is analyzed in detail in the discussion section.

4. Discussion

The process of the DREs in the CMOS inverter is that gamma rays generate much electron-hole pairs in the semiconductor material through the Compton effects. The electron-hole pairs in the PN junction depletion region and a diffusion length of carriers near the depletion region will be collected under the effect of drift diffusion to form the drift diffusion current. At the same time, disturbing the electric potential induces a bipolar amplification effect, which generates a bipolar amplification current. The drift diffusion current and the bipolar amplification current together affect the output of the CMOS inverter. When the input of the inverter is low, the NMOS of the inverter is off and the PMOS is on, the output is high. The output is affected by NMOS drain current.

To analyze the main influencing factors of NMOS drain current, we compare the NMOS drain current with the diodeconnected NMOS which the source and gate of the off-state NMOS are floating as shown in Figure 4. The bipolar amplified current is due to conducting the parasitic transistor. In the diode connection, the source and gate are floating, and the influence of parasitic transistors is removed, and only the diffusion current is drifted. The drift diffusion process is only affected by the generated charge concentration and electric field. Under these two connection methods, the charge concentration and electric field distribution are consistent.

Figure 5 shows the drain current comparison of these two situations. The pulse amplitude of the bipolar amplification current is much larger than the drift-diffusion current. The NMOS electron current density distributions of the inverters after irradiation are shown in Figure 6. As the Figure 6 shows, the main current is the bipolar amplification current



Fig. 4 Schematic diagram of different connection methods of NMOS.



Fig. 5 The current comparison of the NMOS drain in two situations.



Fig. 6 The diagram of NMOS electron current density after irradiation.



Fig. 7 The diagram of the potential comparison of the tangent at $z = 0.05 \,\mu\text{m}$ in Figure 5 in different well structure devices.

form the source to the drain. Therefore, we can conclude the bipolar amplification current of the NMOS is the determinant of the voltage pulse amplitude.

The bipolar amplification current is mainly affected by the well-source junction bias [29, 30], the bipolar amplification current increases with the forward-biased of the well-source junction increasing. Figure 7 shows the potential of the tangent at $z = 0.05 \,\mu$ m in Figure 6 in different well structure devices. As shown in the Figure 7, the well-source junction is in a reverse-biased of 688mV before the irradiation. After the irradiation, the well-source junction is in a forward-biased of 12 mV for DW structure, while the DNW structure is a forward-biased of 3 mV. The result is in complete agreement with the simulation results in Figure 2 and further indicates the bipolar amplification effect is the main mechanism of the DREs in the CMOS inverter.

The bias state of the well-source junction is mainly affected by the generation and collection of the electron-hole



Fig. 8 Schematic diagram of electron-hole pairs generation and collection in DW structure.

pairs in the depletion region of the reverse-biased PN junction. The structure of the device is used to further analyze how the well structure affects the bipolar amplification effect. Because of the small size of the depletion formed by the source and well or drain and well, and the similar effect in the three structures, the reverse-biased PN junction between well structures is the main factor.

Figure 8 shows the generation and collection of the electron-hole pairs in the DW structure. The electron-hole pairs are mainly generated and collected in the depletion region of the P substrate and N well and the P-N junction formed by the P well and N well. Electrons are quickly collected by the N-well under acting the electric field due to fast drifting speed, and the remaining holes raise the potential of the P-well and P- substrate. The remaining holes in the P-well and P- substrate modulate the forward-bias of the well-source junction and affect the bipolar amplification current.

Figure 9 shows generation and collection of the electronhole pairs in the DNW and DPW structures. For the DNW structure, the electron-hole pairs are mainly generated and collected in the depletion region of the PN+ junction formed by P-well and DNW and the PN junction formed by P-well and N-well. According to reference [31, 32], the junction depletion region formed by the well and the substrate will be narrower when the substrate concentration increase, and then the holes collection will be fewer. Electron-hole pairs generated in the depletion region of the PN+ junction are fewer than generated in the depletion region of the P-N junction formed by P- substrate and N well in DW structure. With the doping concentration of the DNW increasing, fewer electron-hole pairs are generated. The fewer electron-hole pairs help to reduce the forward-bias of the well-source junction, which in turn reduces the voltage disturbance. However, DNW isolates the P-well from the substrate, and the forward bias of the well-source junction increases due to the lack of a substrate that shares the remaining holes. These two effects suppress each other, so for DNW, the voltage disturbance is reduced only at high doping concentration.

For the DPW structure, the electron-hole pairs are mainly generated and collected in the depletion region of the P + Njunction formed by DPW and N-well and the PN junction formed by P-well and N-well. Electron-hole pairs generated in the depletion region of the P + N junction are fewer than generated in the depletion region of the P-N junction



Fig.9 Schematic diagram of electron-hole pairs generation and collection in triple-well structures. (a) DNW structure device; (b) DPW structure device.

formed by P- substrate and N well in DW structure. As the doping concentration of the DPW, fewer electron-hole pairs are generated. The fewer electron-hole pairs generated help to reduce the forward-bias of the well-source junction. So for DPW, the voltage disturbance can be effectively reduced, while increasing the doping concentration will significantly increase the suppression effect.

In conclusion, the DREs of the CMOS inverter mainly determined by the bipolar amplification current. Both DNW and DPW structures reduce the forward-bias of the wellsource junction and inhibit the bipolar amplification current by reducing the generation and collection of electron-hole pairs. As the doping concentration of the deep well increases, the stronger the suppression ability. It should be noted the separation of the P-well from the P- substrate by DNW increases the forward-bias of the well-source junction and enhances the bipolar amplification current.

In comparison, SEE and DREs both affect the device through the bipolar amplification effect. For SEE, the well structure only adjusts the influence of the substrate on the well potential. For DREs, the well structure not only adjusts the influence of the substrate, but also forming a reversebiased PN junction and affecting to collect electron-hole pairs.

5. Conclusions

In this article, the effects of the well structure on the DREs has been studied by the 3D TCAD simulation. DPW structure could effectively reduce pulse amplitude of the voltage while the DNW structure reduces the pulse amplitude only in high doping concentration. As the doping concentration of the deep well increases, the pulse amplitude decreases.

Research indicates the different well structures will adjust the number of electron-hole pairs produced by changing the area of the PN junction depletion region, which will affect the final voltage disturbance under the influence of the bipolar amplification effect. The results contribute to the reinforcement design of DREs in CMOS circuits. The use of the DPW structure in bulk CMOS circuits can effectively reduce the DREs. For the DNW structure that has to be used, the doping concentration of DNW needs to be increased as much as possible. Increasing the doping concentration of the deep well can effectively resist the DREs in CMOS circuits.

At the same time, the physical mechanism of traditional SEE is also compared, further revealing the essential difference between the two radiation effects.

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