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Simple and systematic design of FA cell using K map

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Abstract: A simple pass transistor approach using K map is proposed in this communication for design of combinational circuits. The approach is based on switching theory and requires mapping of logic functions into circuit realization using new pass transistor logic style. Low power and small area full adder cell is synthesized which utilized 14 transistors in CMOS implementation.

Keywords: PTL, FA cell, Complementary circuits

Classification: Integrated circuits

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1 Introduction

The syntheses of full adder cells in pass transistor logic are popular as CPL (Complementary pass logic), DPL (Double pass logic) and DVL (Dual Value logic) [1]. A literature survey [2] points out two main approaches to synthesize pass transistor circuits: one- transistor level synthesis based on decision diagrams and [3, 4] second- library–based synthesis [5]. The first approach

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can be applicable to decide for minimum transistor configurations for various gate circuits, which can be suitably used as library for second approach. How to proceed for minimum transistor counts for realizations of the gates is still a problem. This requires consideration of mapping logic functions into circuit realization using different pass transistor logic styles. Karnaugh map representation of a logic function with optimization of the corresponding circuit realization has been in used since a long time but the common rules for simple minimum transistor realizations have yet not been put forward.

The main aim of the work is to develop a simple and systematic method based on transistor level decision approach with K map simplifications for mapping logic functions into circuit realizations. The design rules framed here are utilized in synthesis of a full adder cell which results in realization of 14 transistor full adder cell which is a new circuit and has not been reported earlier to the best of my knowledge. The proposed style of logic synthesis is systematic and requires less number of transistors. This Signal Pass Logic (SPL) Style is simple in application and easy to understand.

2 Proposed Single Pass Logic (SPL) Style

Two switches NMOS and PMOS are used to implement a digital circuit using switching theory. PMOS passes the input signal at logic '0' at its gate and NMOS passes the input on application of logic '1' at its gate. In this proposed SPL approach, the use of complementary signal at the input of the logic function is strictly restricted to avoid the increase of transistors due to use of invertors to complement the signals before applying to control or input of a switch as against in CPL, DPL and DVL. The design rules are summarized under:

1. Cover Karnaugh Map with largest possible cubes (overlapping allowed).
2. Derive the value of a function in each cube in terms of input signals or supply.
3. Don't use the complementary signals at the input or control of the switch PMOS or NMOS. But an invertor can be used if possible at a later stage.
4. Assign one branch of PMOS to each of the cube coverage producing '0' or '1' for a signal value '0'.
5. Assign one branch of NMOS to each of the cube coverage producing '0' or '1' for a signal value '1'.
6. Assign input branch of the transistors to the signal to be passed and control to gate and connect all output branches producing same function to a common node which is the output of the pass transistor network.

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7. To pass complementary signal through a switch, pass the signal first and then complement it using invertor to connect the output to common node.

8. Eliminate the redundant switches by rearrangement.

3 Design of Full Adder Cell

A novel 14 transistor single bit full adder cell is designed using the proposed design rules for SPL. The SUM and CARRY signals of the cell are represented on K map and are given in Table I. The covering of the cubes is made using the proposed design rules.

B Cin A	00	01	11	10
0	0	1 C1	0	1 C3
1	1	0 C2	1	0 C4

(a)

B Cin A	00	01	11	10
0	0	0 C1	1	0 C2
1	0	1 C3	1	1 C4

(b)

Table1: K map for (a)SUM (b) CARRY

For signal SUM, the covering of cubes, show that the pass signal is Cin or Cin' only. The following signal switch arrangement is recommended as per proposed rules:

For C1 : A (0) is gate signal to PMOS, B (0) is gate signal to next PMOS and Cin (0,1) is signal produced.

For C2 : A (1) is gate signal to NMOS, B (0) is gate signal to next NMOS and Cin (0,1) is pass signal and Cin'(1,0) is produced signal.

For C3 : A (0) is gate signal to PMOS, B (1) is gate signal to next PMOS and Cin (0,1) is pass signal to invertor to produce Cin' (1,0) is produced signal.

For C4 : A (1) is gate signal to NMOS, B (1) is gate signal to next NMOS and Cin is pass signal.

It is clear that four switches are sufficient to pass the signals but C1 and C2 are set to pass signal when B = '0' and C3 and C4 are set to pass when

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B= '1'. This requires two switches to set conditions of signal B. As C2 and C3 are producing complementary of pass signal, therefore one invertor is sufficient to produce output for common node. The total of eight transistors is required to produce SUM. The complete circuit for producing SUM signal is given in Fig. 1.

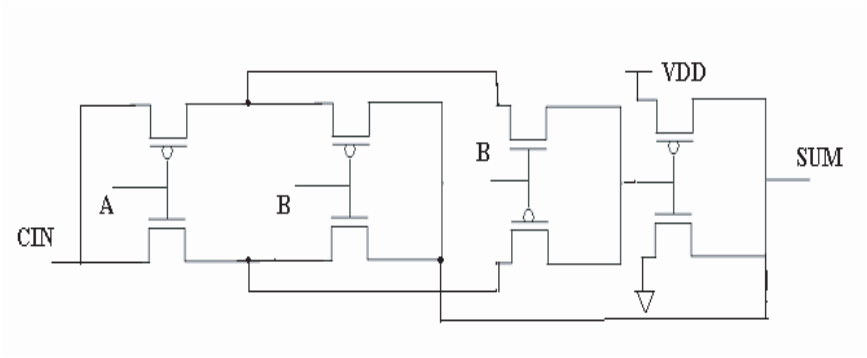

Fig. 1. Sum generating circuit (eight transistors)

For CARRY signal, C1 and C2 coverage shows that the pass signals are B and Cin with conditions of signal B and A. Similar situation is with C3 and C4. Therefore only six transistors are sufficient for CARRY unit as shown in Fig. 2.

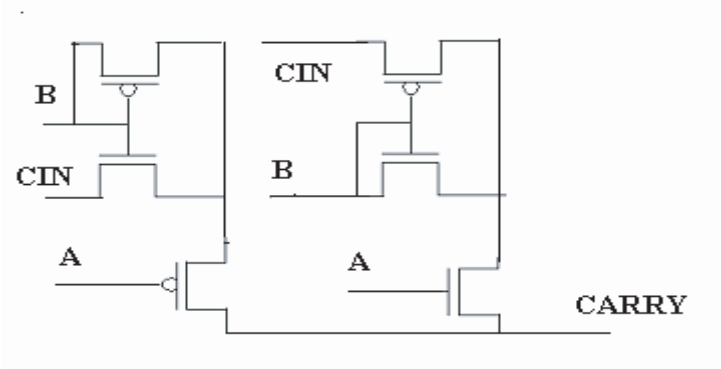

Fig. 2. CARRY generating circuit (six transistors)

4 Discussion

The method presented here is simple and easy to workout for complementary circuits. A novel single bit full adder cell with 14 transistors has been designed and tested on simulation using verilog. The state changes on observable net for input pattern encompassing the entire truth table and run for 40 time unit defined as 10 ns/1 ns. It gives 110 state changes on observable net. SPL gives low power, high speed full adder cell. The speed is lower than that of corresponding CPL adder cell. The signal swing suffers. The number of transistors in SPL can be further reduced to 10 from 14 if three module

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approach is practiced in synthesis of full adder cell using XOR/XNOR and MUX carry configuration. The simulation on Verilog confirms the functional workability of designed full adder cell.

5 Conclusion

The presented design rules have been applied for number for gates including powerless XOR and groundless XNOR circuits and tested for numerous full adder cells. The presented approach is found most general and covers all pass transistor technologies for design with ease and comfort.

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