

A 2/5 mW CMOS $\Delta\Sigma$ modulator employed in an improved GSM/UMTS receiver structure

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Abstract: In this paper, the design of a reconfigurable low-power low-pass Switched Capacitor Delta-Sigma (SC $\Delta\Sigma$) modulator for GSM/UMTS standards used in an optimum low-IF(LIF)/Zero-IF(ZIF) receiver architecture is described. A new approach for obtaining the optimum modulator coefficients is developed which results in relaxed specifications of the circuit components, aggressive noise transfer function (NTF) and a signal transfer function (STF) with the blocker-rejection property. The modulator employs a second/third-order single-stage dual-quantizer structure. It achieves 85.6 dB/57 dB SNDR and -0.2 dBFS/ -0.05 dBFS overload factor at 0.2/2 MHz bandwidth for GSM/UMTS standards and consumes only 2 mW/5 mW from a single 1.8 V supply in a 0.18 μm 1P6M CMOS process. The maximum spread of the modulator capacitors is 105.

Keywords: Delta-Sigma modulator, Capacitor spread, Dual-quantizer

Classification: Integrated circuits

References

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1 Introduction

GSM and UMTS communication standards are the two most commonly used mobile phones from the 2nd and 3rd generations, respectively. To digitize the analog channel signal of these standards with different bandwidth, a reusable,

high linear, high resolution programmable ADC structure must be used. In this paper, a high-order multi-bit SC $\Delta\Sigma$ modulator because of more flexibility and low-sensitivity to clock jitter (in comparison with continuous-time ones) is used for this purpose. A modified LIF(100 kHz)/ZIF(DC) receiver architecture which results in using only one low-pass $\Delta\Sigma$ (LP $\Delta\Sigma$) modulator for GSM is proposed and described in section 2. Through different options for the channel select filter selectivity and the ADC DR, a proper selection based on the minimum power consumption is determined. The optimum $\Delta\Sigma$ modulator structure and the popular approach for obtaining modulator coefficients considering capacitor spread, power and stability constraints are discussed in section 3 and 4. This structure supports both GSM/UMTS standards and has been implemented by SC integrators. The behavioral and transistor-level simulation results obtained by MATLAB and Hspice are explained in section 5. Finally, conclusions and design qualifications are discussed in section 6.

2 The Receiver Back-end Design Trade-offs

The receiver architecture used here is ZIF for UMTS and LIF for GSM. The output spectrums of in-phase and quadrature-phase paths are symmetrical around DC. So, for GSM whose structure is LIF, only the in-phase spectrum after the on-chip SC poly phase filter can be processed in a Low pass $\Delta\Sigma$ ADC and more power is saved in this operation mode.

This P.P.F. acts as image-rejection and to some extent channel select filter centered at 100 kHz for GSM. The ADC's NTF for both GSM/UMTS standards shapes the quantization noise around DC in the 0.2/2 MHz low-pass bandwidth.

It is necessary for both attenuated blocker and desired signal after filtering to be digitized correctly by the ADC residual DR (DR_{res}). The actual required DR of ADC itself is the sum of DR_{res} and some fixed headrooms [3]. Therefore, the power-optimum case depends on the different contributions of analog filter/ADC in BS satisfying. The relation between power of signal (P_{sig}), noise ($P_{n,i}$), blocker (P_{blk}) and blocker signal attenuated by the analog filter with A_{atten} at the ADC input is:

$$DR_{res} = P_{blk} - (P_{sig} + P_{n,i}) - A_{atten}. \quad (1)$$

The approximate baseband power of the receiver is illustrated in Fig. 1 assuming the OTAs are the major source of power consumption. The written numbers bellow or above each data point indicate required filter order corresponding to that frequency offset. So, the worst case power occurs with the greatest filter order and the ADC DR for each case of filter contribution (e.g. 25%, 50% and 75%).

As seen, the optimum case is 25% contribution of the filter in the blocker selectivity (i.e. 75% contribution of the ADC) that imposes about 54.6 dB/41.1 dB DR_{res} , 84/54 dB DR and an analog prefilter of order 2/6 for GSM/UMTS.

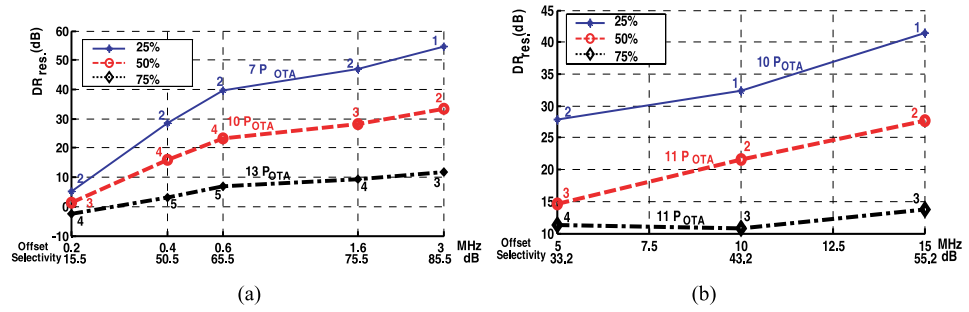


Fig. 1. DR_{res} -blocker selectivity (BS) curve (a) GSM
(b) UMTS.

3 The $\Delta\Sigma$ modulator design procedure

The used modulator in this paper is a 3rd-order single-stage $LP\Delta\Sigma$ with 1-bit and 4th-bit quantizers (dual quantizer technique) which is effective especially for low-OSR, low-voltage, low-sensitive cases [1, 2]. To achieve lower power consumption, the receiver is falling back to a low-power mode with removing one integrator and one bit for GSM. The overload factor of multi-bit modulators is higher than 1-bit ones which cause less power consumption. To overcome the multi-bit DAC nonlinearity and simple circuit implementation, a dual quantizer technique is applied to the standard single-stage distributed-feedback structure. Generally, if the most exterior loop (global feedback) and the most interior loop utilize one-bit and n-bit DAC, respectively, so in an L-order modulator, the (L-2) internal integrators could receive an m-bit DAC where $1 \leq m \leq n$. If the middle loops use less than n-bit DAC, the required swing and power of the integrators are larger and the overload factor degrades. So, all the inner loops in the proposed modulator structure are selected to be n-bit. The required resolution of internal DAC is 8/6 bit for GSM/UMTS. The STF and NTF of the modulator from signal flowgraph of Fig. 2 a can be calculated as:

$$STF = \frac{1}{\Delta} (b_1 c_1 c_2 c_3 h_1 h_2 h_3 + b_2 c_2 c_3 h_2 h_3 + b_3 c_3 h_3 + b_4 (1 + g_1 c_2 h_2 h_3)) \quad (2)$$

$$NTF = \frac{1}{\Delta} (1 + g_1 c_2 h_2 h_3) \quad (3)$$

$$\Delta = 1 + (a_1 c_1 c_2 c_3 h_1 h_2 h_3 + a_2 c_2 c_3 h_2 h_3 + a_3 c_3 h_3 + g_1 c_2 h_2 h_3) \quad (4)$$

Using MATLAB Delta-Sigma Toolbox¹ (DST), all C_i s are one and the output ranges of the integrators are greater than the reference voltage. As it is seen in Fig. 2, a weighted adder is needed before quantizer to realize the position of the STF zeros in the blocker frequency (resulting in image rejection). Since the sum of these weighted coefficients is greater than one, using an active adder, e.g. a gain stage with small feedback factor is necessary which results in some excess power and area dissipation at least in order of one OTA. In this paper, we use a new scaling technique by which STF's

¹Richard Schreier, <http://www.mathworks.com/matlabcentral/fileexchange>

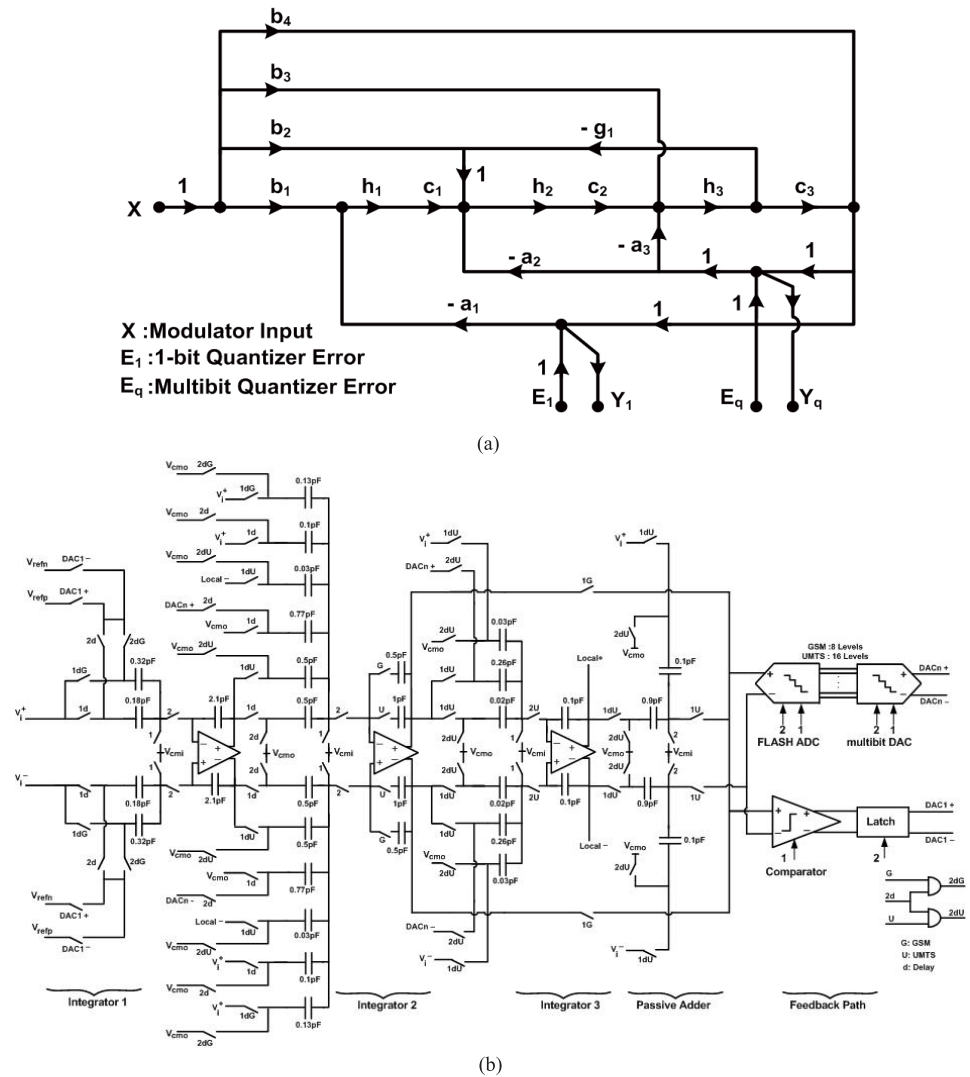


Fig. 2. (a) Modulator's signal flowgraph (UMTS). For GSM mode, $a_3 = g_1 = b_3 = b_4 = 0, c_3 = h_3 = 1$.
(b) Its circuit implementation for GSM/UMTS.

notches (dependent to b_i s coefficients) are achieved properly and the adder is also realized by passive capacitors.

4 The approach to find the optimum coefficients

Assuming that the order of modulator is L , from Eqs. (3) and (4), it is obvious that if all polynomial terms of Eqs. (5) and (6) remain fixed, the gain, poles and zeros of Δ and NTF do not change:

$$\sum_{n=1}^L a_n \prod_{m=n}^L c_m = \text{cte} \quad (5)$$

$$\sum_i g_i c_{i+1} = \text{cte}; \text{ for valid values of } i \quad (6)$$

Also in order to fix STF, the b_i coefficients must be scaled similar to a_i ones. Noting that a scaling factor must be inserted before the b_i s and a_i in the

modulator structure to limit the output swing of the integrators well below the feedback reference voltages. This factor can be found primarily with high-level simulations through a defined swing constraint. Certainly, the small scaling factor relaxes the swing requirement but decreases the modulator SNR since all digital codes of multi-bit DAC did not generate. To use a passive adder, the sum of weighted coefficients before the adder must be one. The maximum spread will be less than a designer defined value named ‘SP’ if the sum of all unrepeated coefficients is equal to product of their minimum, ‘min’, and ‘SP’, so:

$$c_{L-1} + kb_L = 1 \quad (7)$$

$$ka_1 + \sum_{j=2}^L a_j + k \sum_{j=1}^{L+1} b_j + \sum_{j=1}^L c_j + \sum_{j=1}^{[L/2]} g_j = (\text{SP})(\text{min}) \quad (8)$$

Where ‘min’ is a simplified representation for the minimum value of right hand terms. Another effective criteria for determining ‘min’ is power considerations explained next. Mapping of the maximum coefficient spread to the maximum capacitance spread can be accomplished using following relation between absolute capacitor value (C), its 3σ error, the required accuracy of the capacitor in bit number (n) and the ratio between two capacitors (r):

$$C \left(\text{fF}/\mu\text{m}^2 \right) = 0.86 \left(\frac{3u}{3\sigma} \right)^2 = 0.86 \left(\frac{3u}{r} 2^n \right)^2; 0.03 \leq u \leq 0.05 \quad (9)$$

The capacitor accuracy of each modulator stage can be found by system-level simulations with standard predicted coefficients of DST assuming infinite swing for integrators. The maximum required specifications of the reconfigurable modulator are as follow:

$$\text{DC} - \text{gain} = 80 \text{ dB}; \text{ Linearity} = -84 \text{ dB};$$

$$\text{Coefficient matching} = 7.6 \text{ bit}; \text{ Swing} = 0.7 V_{\text{dd}};$$

After scaling according to Eqs. (5) and (6), the new ‘r’ and consequently equivalent value of each capacitance is determined.

In all slew-limited $\Delta\Sigma$ modulators, the first integrator must be settled to full resolution of the ADC. So, to minimizing the current of the first integrator of modulator, the optimum feedback factor ($0 < \beta < 1$) in this stage must be near one particularly for single stage OTAs. Since the errors due to the next stage’s nonidealities are shaped with the preceding integrator stages, the linearity specifications of these stages are relaxed and using smaller β is sufficient. Generally, each β element of feedback matrix ($\beta = [\beta_1 \ \beta_2 \ \dots \ \beta_n]$) with “k” as scaling factor can be written as:

$$\beta_i = \frac{1}{1 + \sum (a_i + kb_i + c_{i-1} + g_{i-1})} \quad \& \quad \beta_1 = \frac{1}{1 + ka_1}; i \leq L \quad (10)$$

From Eq. (10), Eq. (8) can be rewritten as:

$$\sum_{i=1}^L \frac{1}{\beta_i} + L - 1 = (\text{SP})(\text{min}) \quad (11)$$

To use only one sampling capacitor, the STF notches must be determined such that $a_1 = b_1$ and $b_{L+1} < 1$. In this way, the other b_i 's are determined and ' c_{L+1} ' is obtained using Eq. (7). The other coefficients can be found by recursive Eqs. (5), (6), (11) and (11) assuming a specified feedback factor for the first integrator.

5 Simulation Results

The prototype of the SC modulator shown in Fig. 2 is implemented for two different sets of coefficients. One set is obtained by the method described in the previous section with these constraints: ($SP \leq 100$, Max. Swing $\leq 0.8 V_{dd}$, $\beta_1 \geq 0.8$ for both GSM and UMTS). The other set of coefficients were determined through conventional scaling method considering only the output swing of the integrators bellow $0.8 V_{dd}$. The first integrator is realized by telescopic amplifier with less than 1 mW power for sampling rate of 32 MHz corresponding to 80/8 OSR for GSM/UMTS. The remaining stages are realized by a simple differential pair. The STF and the NTF of the proposed modulator before and after optimization are similar as shown in Fig. 3 for UMTS mode. As seen, the STF causes relative rejection of the image/adjacent signals. The SNDR and DR of the modulator are 85.6 dB/57 dB and 89/60 for GSM/UMTS. To have the same DR before and after applying optimization method, some OTAs with higher power must be used. As an example, for $\beta_1 = 0.92$ (0.8) in the modified coefficient set, the power consumption and "SP" are about 5 mW(2 mW) and 105(21) for UMTS(GSM), respectively. Whereas using the conventional coefficient set, the power consumption and "SP" are about 9 mW(5 mW) and 300(93) for UMTS (GSM) assuming the same SNR and DR in both modified and conventional cases. The modulator's output spectrum is shown in Fig. 3 assuming the same OTAs (and consequently same power consumption) are employed before and after coefficient optimization. The SNDR improvement is 10 dB after optimization.

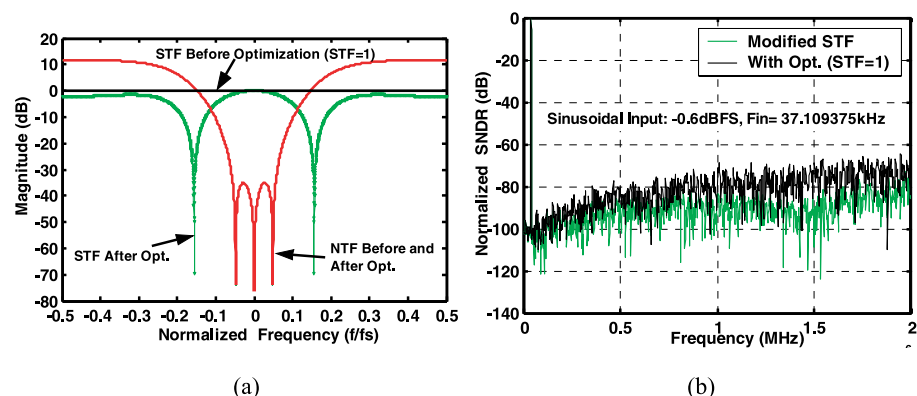


Fig. 3. (a) The modulator's STF and NTF for UMTS mode and (b) its output spectrum.

6 Conclusions and Design Qualifications

In this paper, a new approach to find the optimum coefficients of a $\Delta\Sigma$ modulator considering some practical constraints is developed. Using this method, the power and maximum capacitor spread is improved relative to the conventional method assuming specified performance. The reliability of the proposed method is verified by a reconfigurable modulator implemented in a SC structure with a $0.18\ \mu\text{m}$, $1.8\ \text{V}$ 1P6M CMOS process. The designed modulator can be used as a baseband building block in a GSM/UMTS receiver. The modulator consumes less power (about 50%) and has very low sensitivity to the clock jitter unlike the previously continuous-time modulators such as [1] and [2].²

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