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Reliable detection of CMOS stuck-open faults due to variable internal delays

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Abstract: Testable designs for detecting single stuck-open faults in CMOS circuits have been proposed so that the tests remain valid even in the presence of unequal delays in the circuit. Existing approaches require the CMOS gate to be internally modified and are thus suitable for future chip designs. This paper proposes two versatile designs that can be adapted for both existing chips and new chip designs. A 3-sequence test set and a 2-sequence test set are derived for the proposed designs to reliably detect stuck-open faults.

Keywords: stuck-open faults, design-for-testability, CMOS circuits

Classification: Integrated circuits

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1 Introduction

As the complexity of CMOS circuits increases, test generation and fault simulation become increasingly difficult and challenging. In order to test CMOS integrated circuits, manufacturers and consumers have largely relied on stuck-at-zero and stuck-at-one fault models. While stuck-at-fault models are adequate in modeling many physical failures, it has been shown that certain physical failures are technology dependent and stuck-at-fault models are inadequate especially for CMOS circuits [1].

An open or a break at the drain or source of a MOSFET gives rise to a class of non-conventional failure called stuck-open faults. If a stuck-open exists, a test vector may not always guarantee a unique repeatable logic value at the output because there is no conducting path from the output node to either V_{DD} or V_{SS}. The output depends on the previous logic value stored in the output node capacitance and causes a combinational circuit to emulate a sequential circuit making testing extremely difficult. To solve this, it is necessary to first apply an initializing input test vector to set the output to a known state. A second test vector is then applied to sensitize the path through the MOSFET to be tested. If the output changes to its complementary state, then a stuck-open fault is not present. If on the other hand, the output does not undergo a change in state, then a stuck-open fault is detected.

2 Prior work and problem description

Several approaches for testing stuck-open faults in CMOS combinational circuits have been proposed in the literature [2, 3, 4, 5, 6, 7] and are reviewed in [5]. But recent studies [7, 8, 9] have shown that when the initializing vector T1 is applied to set the output to a known state and is changed to test vector T2, it is possible that during the transition, all input variables may not change at the same time. Variable delays in the input and along different paths in the circuit can spuriously complement the initialized output state, thereby rendering it impossible to reliably detect a stuck-open fault.

The problem is illustrated using an AND-OR-INVERT CMOS gate. Fig. 1 a shows the general structure of CMOS circuit and Fig. 1 b shows the circuit details at the transistor level. The CMOS circuit consists of a network of p-channel MOSFETS (PFETs) and a network of n-channel MOSFETS (NFETs). The internal configuration of the PFETs and NFETs are dual in structure. Also, every input is connected to both a PFET transistor in the PFET network and its corresponding dual in the NFET network. In order to detect if MOSFET P1 is stuck-open, any of the following initializing vectors can be applied: T1 (ABCD) = (0011) or (1100) to set the output node to logic 0. Test vector T2 (ABCD) is chosen such that the output changes to logic 1 if the circuit is fault-free or retains its previous value of logic 0, if a stuck-open fault is present. The following test vectors: T2 (ABCD) = (0110) or (0101) satisfy the above requirements. When changing from initializing vector T1 = (0011) to test vector T2 = (0110), inputs B and D undergo a

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change. If input D changes before input B, then T1 = (0011) changes momentarily to (0010) causing the output node to spuriously charge to logic 1 through transistors P2 and P4. When the test vector T2 stabilizes to (0110), the stuck-open fault in transistor P1 will not be detected because the output would have already changed its state indicating that the circuit is fault-free.

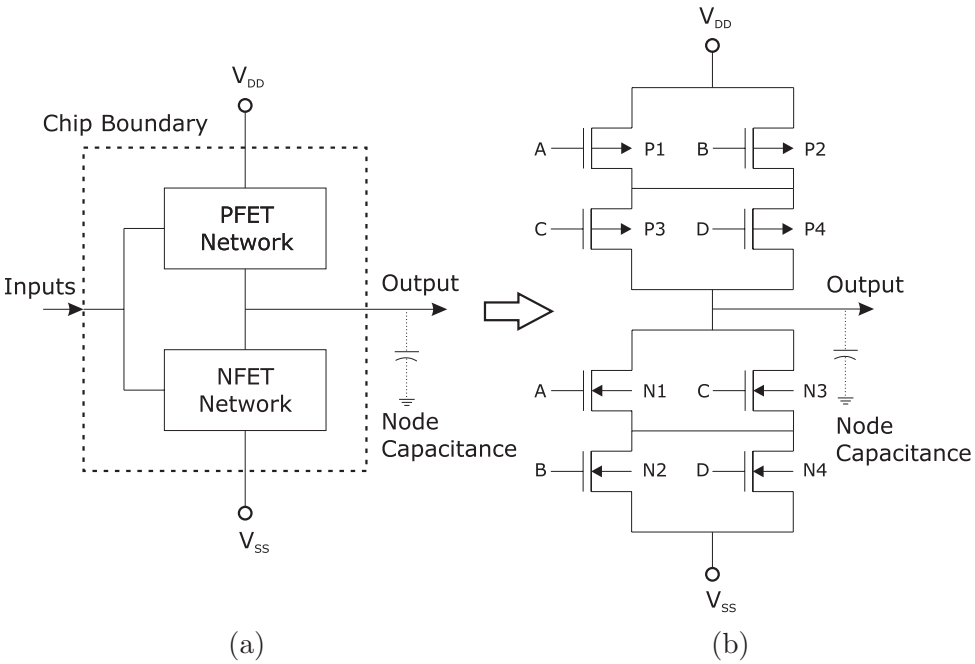

Fig. 1. (a) General structure of CMOS gate (b) Circuit details of CMOS gate

The solutions that have been proposed to reliably detect stuck-open faults in the presence of variable delays are to design the entire chip for testability by adding MOSFETs internally. In this paper, it is shown that existing CMOS chips can be tested for stuck-open faults by using MOSFETs external to the chip without the need to redesign the original chip. The approach can also be used for internal designs. Two implementations are presented in the next section and the test vectors are derived for each design.

3 Proposed approaches to detect stuck-open faults

Modification 1: The original CMOS circuit is augmented with two transistors, PFET-1 and NFET-1 as shown in Fig. 2. The design is versatile and can be implemented with existing chips or can be designed for testability in new chips. PFET-1 and NFET-1 are specifically designed to prevent any transitory spurious charging of the output node capacitor that occurs due to internal delays. To detect a stuck-open fault in a PFET network, the output node capacitor is first set to logic 0 through one or more conducting NFETs from V_{SS}. A second test vector then creates a conducting path from V_{DD} through the PFET under test to the output node. Likewise, to detect a stuck-open fault in an NFET network, the output node capacitor is set to

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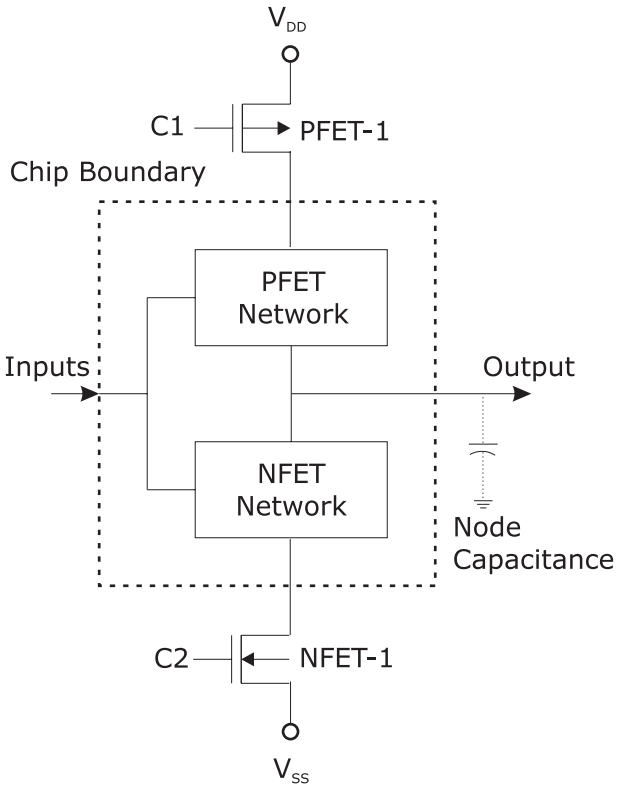

Fig. 2. Modification 1 to detect stuck-open fault

logic 1 through one or more conducting PFETs from V_{DD}. A second test vector then creates a conducting path from V_{SS} through the NFET under test to the output node. The added FETs are controlled by inputs C1 and C2.

Test vector generation: A test vector is made up of inputs I, C1 and C2. T= [I, C1, C2] where I is the set of inputs that turn appropriate transistors ON or OFF to create a path for initializing or for testing, and C1 and C2 are the control signals of the added transistors. Let T_P denote any combination of transistor inputs that creates a conducting path from V_{DD} to the output. The output node is initialized to logic 1. Let T_N denote any combination of transistor inputs that creates a conducting path from V_{SS} to the output. The output node is initialized to logic 0. Let T'_P denote a specific combination of input that creates a conducting path from V_{DD} to the output through the transistor that is tested for stuck-open fault and let T'_N denote a specific combination of input that creates a conducting path from V_{SS} to the output through the transistor that is tested for stuck-open fault.

To detect if a PFET or NFET is stuck-open, a sequence of three test vectors, T1, T2, and T3 is required. Test vector T1 initializes the output to logic 0 or logic 1. Test vector T2 controls inputs C1 and C2 of the FETs to isolate all FETs from both V_{DD} and V_{SS}. This prevents any spurious changes from occurring at the output node due to a momentary conducting path from either V_{DD} or V_{SS}. At the same time a test vector T'_P or T'_N is applied to detect a stuck-open fault of a specific PFET or NFET under test respectively. Test vector T3 now permits the output node to change if the

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PFET or the NFET is fault-free or retain its initialized value if a stuck-open fault exists. The sequence of three test vectors ensures that only one control input changes at any time thereby preventing the possibility of a spurious conducting path to change the initialized value of the output node.

The 3-sequence test vector that is guaranteed to detect single stuck-open faults in the PFET network, NFET network and the added circuitry are derived. The sequence T1 = [T'_N, 1, 1], T2 = [T_P, 1, 0], and T3 = [T_P, 0, 0] detects stuck-open fault in a PFET. The sequence T1 = [T'_P, 0, 0], T2 = [T_N, 1, 0], and T3 = [T_N, 1, 1] detects stuck-open fault in a NFET. For the added PFET-1, the sequence T1 = [T'_N, 1, 1], T2 = [T'_P, 1, 0], T3 = [T_P, 0, 0] detects a stuck-open fault and for the added NFET-1, the sequence T1 = [T'_P, 0, 0], T2 = [T'_P, 1, 0], T3 = [T'_N, 1, 1] detects a stuck-open fault.

Modification 2: The original CMOS circuit is augmented with four transistors, PFET-1, PFET-2, NFET-1 and NFET-2 as shown in Fig. 3. This design can be implemented on existing chips and integrated in new chip designs. Note that there are only two control signals. The addition of four FETs and control signals C1 and C2 reduces the 3-sequence test vectors to 2-sequence test vectors. The reduction is possible because test vector T1 initializes the output node by using PFET1 and PFET2 or NFET1 and NFET2. It also applies the input test vector to detect a stuck-open fault in either the NFET or the PFET network respectively. Test vector T2 sensitizes the path from the FET under test to the output.

Test vector generation: The 2-sequence test vector that is guaranteed to detect single stuck-open faults in the PFET network, NFET network, and

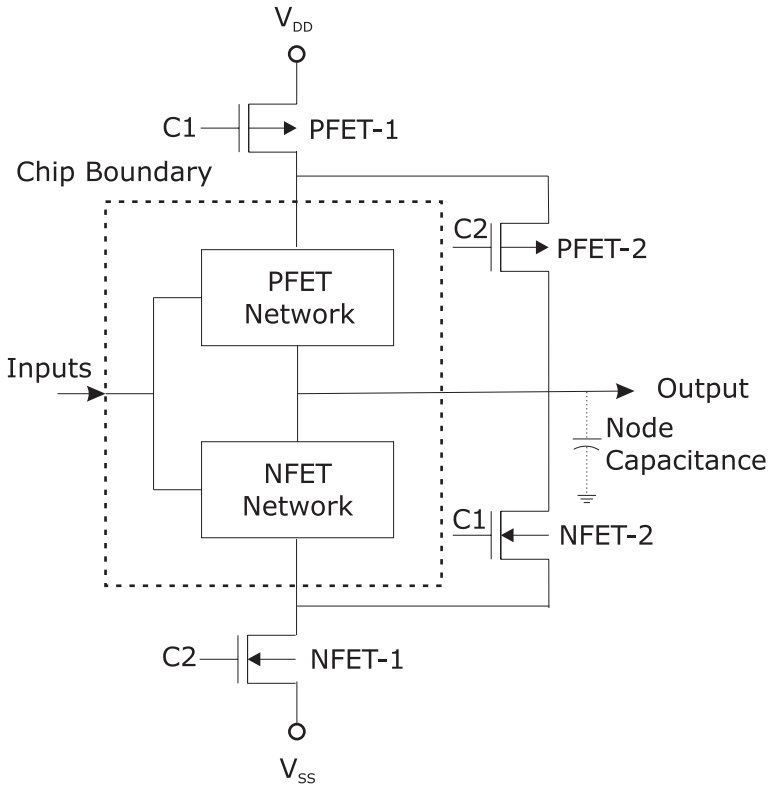

Fig. 3. Modification 2 to detect stuck-open fault

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the added circuitry are presented. The sequence T1 = [T_P, 1, 1] and T2 = [T_P, 0, 1] detects stuck-open fault in a PFET. The sequence T1 = [T_N, 0, 0] and T2 = [T_N, 0, 1] detects stuck-open fault in a NFET. For the added PFETs, the sequence T1 = [T'_P, 1, 1] and T2 = [T'_P, 0, 1] detects a stuck-open fault in PFET-1, and the sequence T1 = [T'_N, 0, 1] and T2 = [T'_N, 0, 0] detects a stuck-open fault in PFET-2. For the added NFETs, the sequence T1 = [T'_N, 0, 0] and T2 = [T'_N, 0, 1] detects a stuck-open fault in NFET-1, and the sequence T1 = [T'_P, 0, 1] and T2 = [T'_P, 1, 1] detects a stuck-open fault in NFET-2. The placement of the FETs as shown in Fig. 2 and Fig. 3, also guarantees that the output node will remain a logic 0 or logic 1 independent of arbitrary delays within the circuit.

4 Conclusion

In irredundant CMOS gates where stuck-open faults cannot be detected due to delays in the circuit, design-for-testability techniques have been proposed. Previous solutions focused on the design of new CMOS gates with internal changes designed for testability. This limited the possibility of detecting stuck-open faults in existing CMOS gates that are widely prevalent. The two designs presented in this paper offer a viable solution to test stuck-open faults in CMOS gates. The design is versatile compared to existing solutions because it can be adopted for both new chip designs and existing chips. It is shown that using the 3-sequence and 2-sequence test vectors, it is possible to reliably detect stuck-open faults even in the presence of arbitrary delays and the inherent output node capacitance.

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