ELectronics EXpress

IEICE Electronics Express, Vol.2, No.18, 482–487

A new active pixel structure with a pinned photodiode for wide dynamic range image sensors

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Abstract: A wide dynamic range CMOS image sensor based on a new active pixel structure with a pinned photodiode is proposed and evaluated with device simulations. The proposed pixel device has a linear and a logarithmic characteristics in low and high illumination region, respectively. The technique of direct detection of photodiode potential leads to a wide logarithmic response compared with the conventional linear-log wide DR image sensor with pinned photo diode.

Keywords: CMOS image sensor, wide dynamic range, floating gate

Classification: Photonics devices, circuits, and systems

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DOI: 10.1587/elex.2.482
Received August 11, 2005
Accepted August 22, 2005
Published September 25, 2005

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1 Introduction

Recent developments of cameras for automobiles require very wide dynamic range (DR) image sensors with more than 100 dB. A consumer grade CMOS image sensor, however, has a dynamic range of typically around 60 dB.

Dynamic range of an image sensor is defined by the ratio of the saturation signal level to the noise level [1]. It is well known that the dynamic range of CMOS image sensors can be expanded by using a detector producing a logarithmic response to the light intensity [2]. However, such a logarithmic response detector has a response time inversely proportional to the light intensity. This causes a severe image lag [3]. This problem can be solved by using a detector that has a linear and a logarithmic responses for low illumination and high illumination level, respectively [4]. In wide DR image sensors with logarithmic or linear-logarithmic responses, in order to expand the dynamic range to the low illumination level, a pixel structure with pinned photodiode [5] should be employed. The pinned photodiode structure can reduce the dark current significantly, and the reset noise can be canceled by in-pixel charge transfer and correlated double sampling (CDS) at the column readout circuit [6]. Recently, an active pixel sensor with pinned photodiode and in-pixel charge transfer has been reported [4]. However, in this structure reset and signal levels of the floating diffusion will be varied during the readout operation if the light intensity level is very high. This causes a complicated non-linearity in the photo-conversion curve.

This letter proposes a new active pixel structure with pinned photodiode and direct detection of the photodiode potential using a floating gate structure. The outstanding benefit of the proposed pixel structure compared to the conventional active pixel with the pinned photodiode is that the read signal and reset level are stable during readout operation because our device directly detects the photodiode potential with the floating gate.

2 Pixel structure and operation principle

Figure 1 (a) shows a proposed pixel structure. A unit pixel consists of a photodiode, a transistor M_1 for draining photo-generated charge, a floating gate (FG), a transistor M_2 to initialize the floating gate, a pixel amplifier M_3, and a row selection transistor M_4. In this structure, the surface under the silicon di-oxide is pinned by holes during the photo signal accumulation to reduce the electron generation by interface states located at $Si - SiO_2$ interface. This greatly reduces the dark current [5]. Each impurity concentration is elaborately controlled so that accumulated charges in the photodiode are completely removed in the reset operation. This can be verified from the simulated potential distribution which is shown in the section of the simulation result.

Designed pixel is utilizing the method that detects the potential variance of a photodiode without performing charge transfer to a charge detection element such as a floating diffusion. The floating gate is used for detecting the amount of charges generated by incident light.

DOI: 10.1587/elex.2.482
Received August 11, 2005
Accepted August 22, 2005
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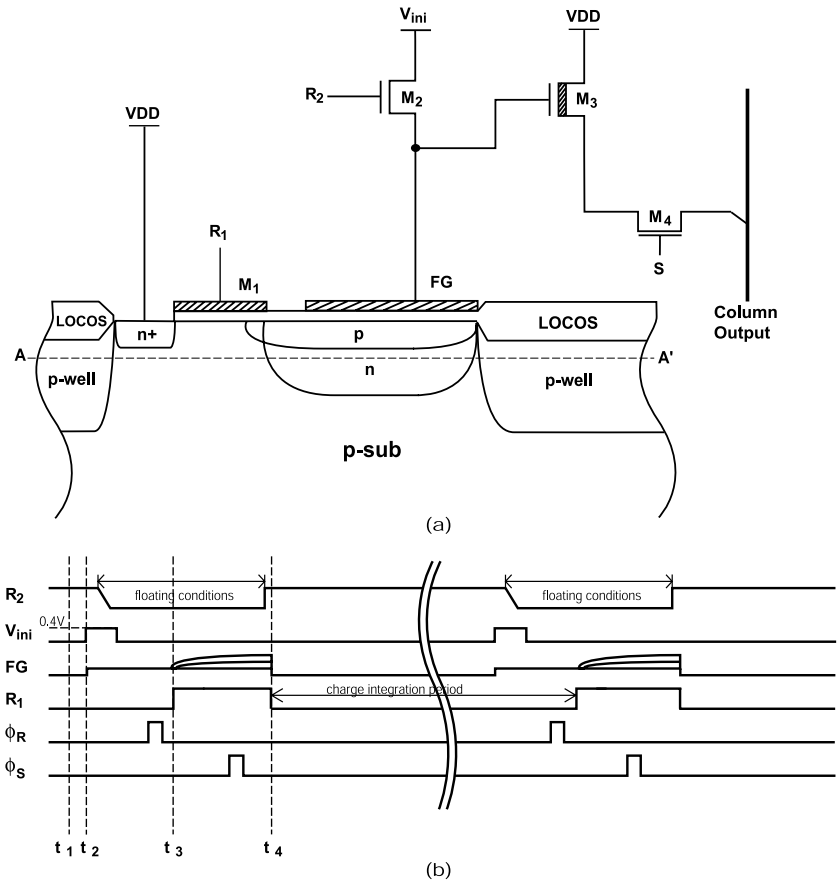

Fig. 1. Operating principle of the designed pixel: (a) pixel structure (b) timing diagram

The timing diagram is shown in Figure 1 (b). The signal charges generated by incident light are collected during the charge integration period. The potential of the n region of the photodiode is decreased as photo-generated charges in the photodiode are accumulated. Before signal charges are read out, the floating gate is set to the pre-determined bias voltage at time t_2. The pinned region under the FG must be depleted by applied bias voltage before signal readout and the maximum output swing of the pixel is determined by it. Therefore, the pre-determined bias voltage is set to $0.4\,V$ which satisfies above two conditions. A depletion type MOSFET is used for pixel source follower to readout low level initial voltage. The initialization transistor M_2 is then turned off. As a result, the floating gate, FG, goes to floating condition. This initial voltage can be used for reset level in a CDS operation. At time t_3, the reset signal, R_1, is activated to remove photo-generated charges in photodiode. In this reset operation, accumulated charges are transferred completely from the photodiode to the drain of reset transistor. Therefore, reset noise induced by the remained signal charges in photodiode is cancelled. In the reset operation, a potential variance of the floating gate, FG, is proportional to the amount of accumulated charges. This signal voltage in the FG is used for signal level of the CDS operation.

If the accumulated charges exceed the maximum well capacity in a certain integration time, the charges accumulated in potential well begin to overflow

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to the drain which is connected to VDD, and the potential increases logarithmically like a subthreshold operation of MOSFET in weak inversion. As a result, the proposed sensor has a linear response to low illumination and a logarithmic response in high illumination region. Using this technique, the dynamic range of the proposed pixel can be extended to more than $120\,dB$ which is verified from the device simulation in the next section.

3 Simulation results

In order to confirm the performance of the designed sensor, device simulation was carried out with the proposed pixel structure shown in Figure 1 (a), excluding the selection switch, M_4, and the pixel amplifier, M_3. To obtain precise conversion gain of the sensor, the parasitic capacitance of the transistor M_3 and M_4 is calculated and added in the FG node.

3.1 Potential distribution

In the proposed pixel structure, it is important to achieve both of the perfect charge transfer and making the surface of silicon to be accumulated by holes during charge accumulation. Figure 2 (a) and (b) show a simulated potential distribution of the designed sensor in reset phase and charge accumulation phase, respectively. In the reset phase, there is no potential barrier between the photodiode and the n^+ drain as shown in Figure 2 (a). It is clear that accumulated charges in photodiode are completely transferred to the drain. Therefore, reset noise that results from the variance of remained signal charge after reset operation is reduced. In the charge integration period, the surface potential is maintained to $-0.2\,\mathrm{V}$ as shown in Figure 2 (b). As a result, the surface under the SiO_2 is accumulated by holes, resulting in dark current reduction. Figure 2 (c) shows the potential distribution corresponding to each control signal of timing diagram of Figure 1 (b). From this result, it is clear that accumulated charges are completely transferred to the drain at the reset phase t_3.

3.2 Output characteristics

Accumulated charge to voltage conversion efficiency is an important parameter which determines the sensor characteristic. In the proposed pixel structure, a floating gate is used to convert a photoelectron to signal voltage. Charge to voltage conversion characteristic was confirmed using a device simulation. The output voltage responds linearly to photo-generated charge up to $400\,mV$ as shown in Figure 3 (a). Therefore, the maximum charge capacity that can be accumulated in the photodiode with a linear increase is 11000 electrons with the floating gate area of $10\,\mu m^2$, if the resulting conversion gain is $36\,\mu V/e-$.

A linear-logarithmic response of the sensor in which the sensor response turns linear to logarithmic at the boundary of light intensity is shown in Figure 3 (b). It is confirmed that collected charge is saturated at the light intensity of $0.03\,W/cm^2$ and begins to increase logarithmically as the light

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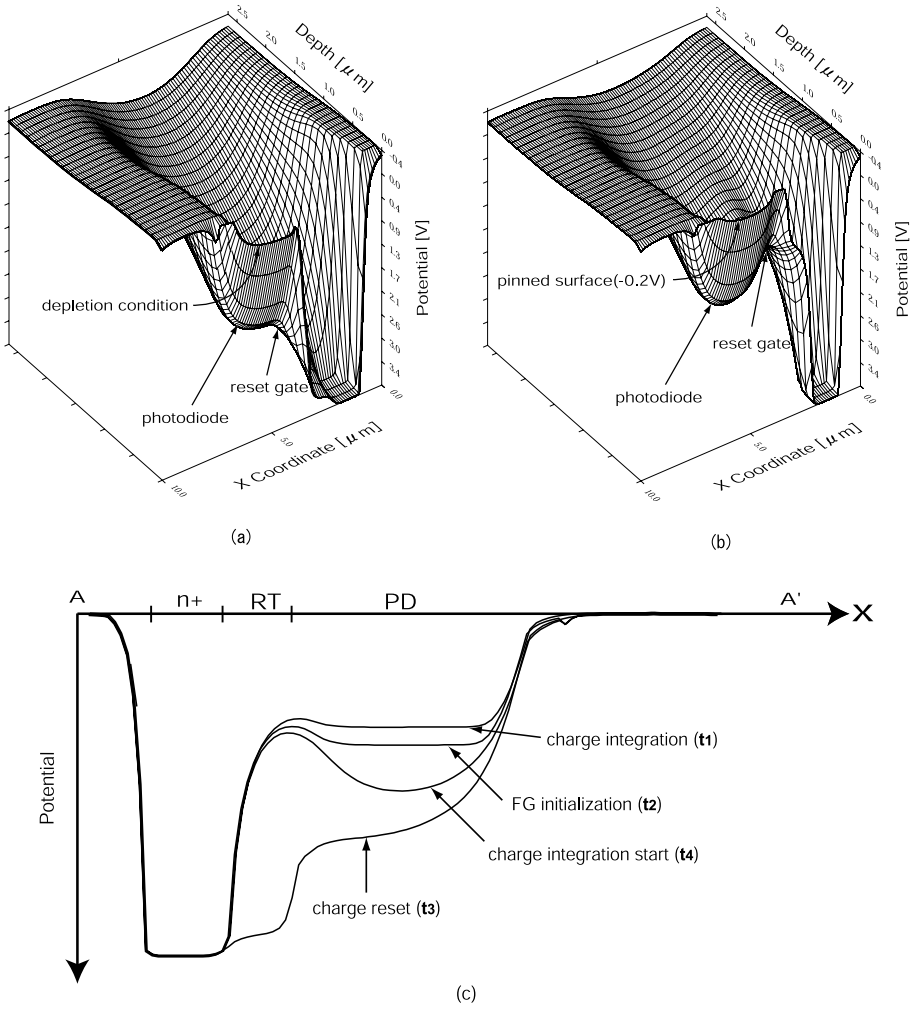

Fig. 2. Potential distribution of the proposed pixel: (a) Reset phase (b) Charge accumulation phase (c) Potential profile for each control signals

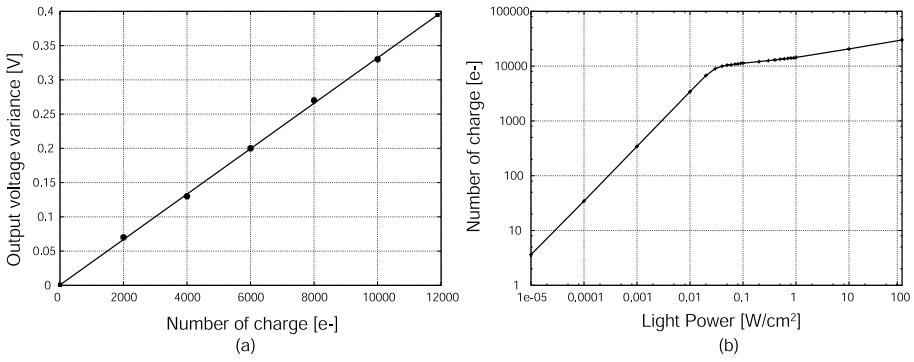

Fig. 3. Simulated results of the proposed pixel: (a) charge to voltage conversion characteristic (b) linear and log response of the designed sensor

illumination increases. Each of the linear and logarithmic response covers three and half decades of light intensity, and the resulting dynamic range is $140\,dB$.

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4 Conclusion

A new pixel structure for extending the dynamic range of CMOS image sensors as well as achieving low-noise characteristics is presented. The floating gate detection of photodiode potential variation due to incident light has a linear-logarithmic response, and the resulting dynamic range can be extended to more than 120 dB according to the device simulation. The important properties of the pinning of $Si - SiO_2$ interface during charge accumulation and complete charge draining, which are essential property for low-noise pixel have been confirmed by simulations.

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