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Power Valve: for low power operation and low stand-by power

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Abstract: The concept of Power Valve is presented. It consists of power switch transistors and control circuits, which give variable impedance to the power supply. The circuit controls the internal power supply voltage of logic circuits and reduces the voltage swing of signals. An experiment using a 130-nm test chip showed a 36.0% operating power reduction for a 16-bit multiplier at 50 MHz. The Power Valve can be designed using logic transistors, with the same leakage current to the circuit which have IO transistor switch.

Keywords: Power switch, switch transistor, low power, leak current

Classification: Integrated circuits

References

[1] T. Douseki, S. Shigematsu, J. Yamada, M. Harada, H. Inokawa, and T. Tsuchiya, "A 0.5 V MTCMOS/SIMOX logic gate," *JSSCC*, vol. 32, no. 10, pp. 1604–1069, Oct. 1997.

[2] T. Inukai, M. Takamiya, K. Nose, H. Kawaguchi, T. Hiramoto, and T. Sakurai, "Boosted Gate MOS: Device/circuit cooperation scheme to achieve leakage-free Giga-scale integration," *CICC*, pp. 409–412, 2000.

[3] T. Yamashita, T. Fujimoto, and K. Ishibashi, "Switch transistor techniques for both low stand-by power and low power operation," *Tech. Rep. IEICE*, SDM2004-141, ICD 2004-83, pp. 7–12, Aug. 2004.

[4] T. Ishihara and K. Asada, "A system level memory power optimization technique using multiple supply and threshold voltages," *Proc. ASP-DAC*, pp. 456–461, 2001.

[5] M. Johnson, D. Somasekhar, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS," *IEEE Trans. VLSI Syst.*, vol. 10, no. 1, pp. 1–5, Feb. 2002.

[6] M. Hashimoto and H. Onodera, "Increase in delay uncertainty by performance optimization," *IEICE Trans. Fundamentals*, vol. E85-A, pp. 2799–2802, Dec. 2002.

[7] V. Gerousis, "Design and modeling challenges for 90 nm and 50 nm," *CICC*, pp. 353–360, Sept. 2003.

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1 Introduction

As technology scales down, leakage current such as sub-threshold and gate leakage become a serious problem. To reduce the leakage current in stand-by mode, some researches have been reported switch transistor techniques, such as MTCMOS [1] or Boosted-Sleep [2].

MTCMOS assumes a multi-Vth process and implements a switch with a high-Vth transistor. Unfortunately this approach increases the die area and wafer cost. Boosted-Sleep also takes up a large area for the switch transistor with thick gate-oxide and charge pump circuitry.

We propose to control the power transistor so that it acts as a variable impedance device, rather than switch transistor [3]. Since we can use a narrower gate width for the Valve Transistor, it occupies less area than the conventional switch transistor techniques. Since the Valve Transistor reduces the internal supply voltage, the operating power is reduced.

There are many circuit blocks in an SoC. The chip operates to meet the required operation speed. However, not all circuit blocks have to operate at the highest speed. When the propagation delay has margin to its required speed, power can be saved by decreasing the supply voltage.

Dynamic Voltage Scaling (DVS) [4] can reduce power by lowering the clock frequency. However, the DVS technique requires a DC-DC converter to control supply voltage. Thus, it is impractical to apply DVS to many blocks in the LSI. The Power Valve, on the other hand, is a simple technique and can provide a proper supply voltage to each circuit block.

It is difficult to apply the optimal operating voltage to each circuit block in the LSI; however, Power Valves can be used in each circuit block. It is not practical to feed individual VDDs to each block. Power Valves can provide power to every block to reduce operating power.

2 Power Valve operation

2.1 Circuitry of Power Valve

There are actually two types of Power Valve, as shown in Figure 1 (left). In PV-1, a small-gate-width transistor is used. It operates like a series resistor, which allows to rise VGND voltage. The current of the logic circuit flows into the Power Valve. The current raises the VGND level with the impedance of the Valve Transistor. The raised VGND reduces the signal voltage of the logic gates, which reduces operating power. Some PV-1 transistors can be used in parallel, to achieve some operating speeds. For faster operation such as multimedia or game operation, large sized transistor should be turned on to guarantee the operation speed. For slower speed operation such as text processing or key input waiting, only a small transistor should be on to reduce operating power.

PV-2 has series stacked transistors. The stacking effect [5] is known to reduce leak current. In the next section, we show that the leakage of a stacked logic transistor is as low as that of a thick-oxide transistor.

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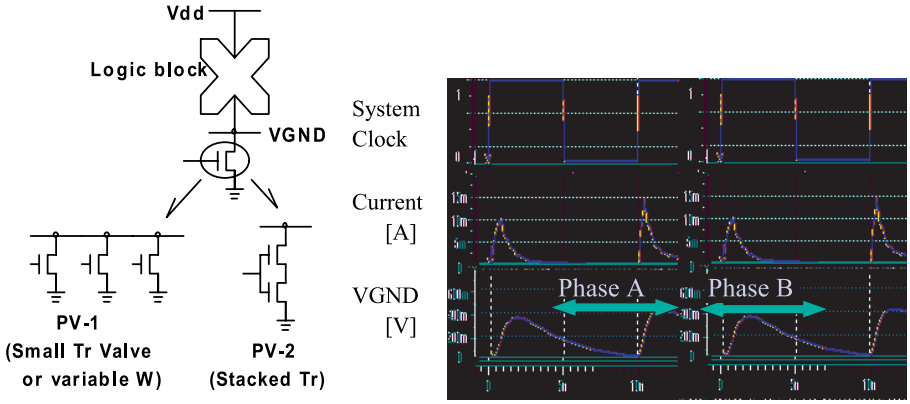

Fig. 1. The concepts of Power Valve (left) and simulated waveforms of power supply current and VGND voltage (right). In phase A, toggles occur in the higher density. VGND is then raised with higher impedance by using PV-1.

The two types of Power Valve can be used in combination. Stacked small transistor enables low power operation and low stand-by leak.

2.2 Power Valve in operation mode

Figure 1 (right) shows current waveforms of a 16×16 bit multiplier circuit. The power supply current rushes into the circuits when the clock cycle begins, because most paths are usually much shorter than the critical path [6]. With PV-1, the VGND voltage follows the current waveform. At the beginning of the clock cycle, many gates toggle. As the Valve Transistor acts like a resistor and VGND goes up (phase "A" in Figure 1), power consumption is effectively reduced in this phase, because of the smaller signal voltage. In the phase "B," power is consumed only for longer paths, including the critical path. During this phase, the VGND voltage goes down to ground level. The supply voltage is thus maximized, so the critical path can operate at the designed speed.

There is no need to use a level shifter while signal voltage is transiently reduced. Signal voltage becomes full swing in the latter part of the system clock cycle.

2.3 Low stand-by power with logic transistor switch

We propose a power switch technique to reduce leakage power in stand-by mode using a stacked switch transistor of a single Vth process. The single Vth process lowers the wafer cost, and eliminates the IO transistor to reduce the layout area penalty.

Conventionally, high-Vth transistors or thick-oxide transistors have been used as the power switch to cut off leak current. We employed a logic transistor with a small gate width.

Figure 2 shows simulated transistor leak current versus gate width for 130-nm CMOS technology. Three types of transistors are shown, logic, stacked

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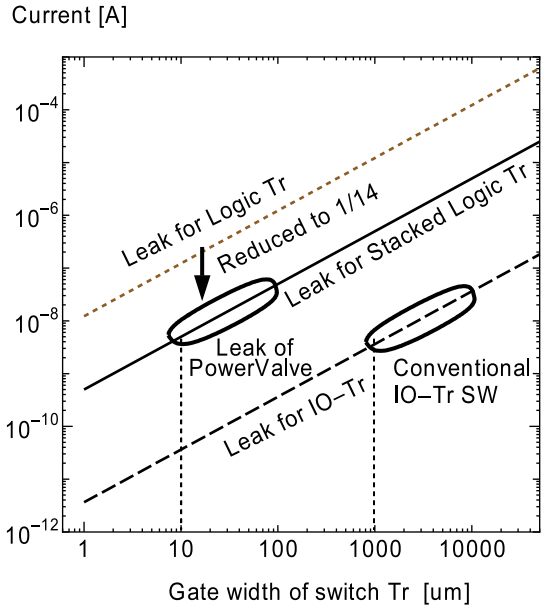

Fig. 2. Leak currents of logic, stacked logic, and IO transistor. The conventional switch transistor leak is represented by the circled parts of IO-Tr leak curve. The Power Valve transistor consists of stacked logic transistors. The Power Valve leakage is comparable to that of the conventional SW, because the gate has a small width and is stacked.

logic and IO transistor. Logic transistor is assumed for a low-Vth high-performance transistor. IO transistor is for 3.3 V IO transistor here.

A conventional thick-oxide transistor switch would have 1/10th the width of the total logic gate width [1], for example, 1 mm to 10 mm for 3 k to 30 k gates of logic. In this case, leakage current will be 40 nA to 400 nA. By replacing the switch transistor with a logic transistor, "on" current increases by 10.3 times, from 59.5 uA/mm for an IO transistor to 618 uA/mm for a logic transistor at Vgs = 1.2 V. Thus, the gate width can be resized to 1/10.3. However, leak current increases by 1140 times at the same gate width, from 59 pA/um for the IO transistor to 4.14 uA/um for the logic transistor. Even considering that the gate width can be resized to 1/10.3, leakage current is still 110 times higher than in the conventional design.

Using PV-1, the required drive current can be reduced to about 1/10th that of conventional design, which is 10 um to 100 um of gate width for a logic transistor. Through the stacking effect of PV-2, leak current can be reduced to 1/14. Combining PV-1 and PV-2, leakage current can be reduced up to 1/1400 compared with the logic transistor switch.

Even using the logic transistor, the stacked transistor can make the leakage comparable to the conventional thick-oxide switch transistor. We can achieve the same or smaller leakage as that of the conventional IO transistor switch by applying the Power Valve.

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3 Test chip implementation

We fabricated a test chip using 0.13-um CMOS technology. We implemented four-parallel 16-bit multipliers as a logic block. Figure 3 (upper) shows a photograph of the chip. Size of the multipliers is for 170-um × 445-um, which is shown in the red dashed-line. Area for the switch transistors including PV-2 feedback circuit is for 10-um × 40 um, which is shown in the blue circle. Area penalty is 0.5%.

Figure 3 (left) shows the measured supply current versus operating frequency. The 5-um and the 25-um transistor curves are for PV-1. The 5-um Power Valve shows a 36.0% power reduction at 50 MHz compared with the circuit without any switch transistor. The reduction of the PD product shows that Power Valve effectively reduces operating power.

Figure 3 (right) shows the propagation delay of the multiplier. The 25-um width PV-1 is 1.43 times slower than the non-switched simulated reference at 1.2 V. The 5-um PV-1 is 2.86 times slower.

We have thus shown that we can reduce operating power by controlling the Power Valve, when the circuit block can handle an extra delay penalty.

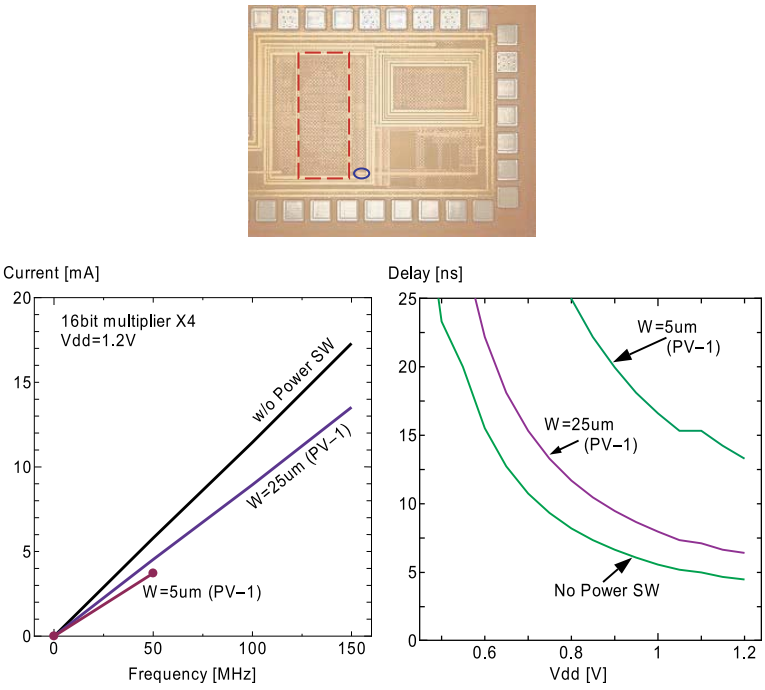

Fig. 3. Chip micrograph, measured supply current and propagation delay.

4 Conclusion

We explained the concept of Power Valve. A Power Valve consists of power control transistors and control circuits, which give variable impedance for the power supply. A 130-nm test chip measurement showed that it delivers a 36.0% power reduction to 16-bit multipliers operating at 50 MHz.

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The Power Valve can also be designed using logic transistors, with the same leakage current to the circuit as an IO transistor switch. It reduces the area and cost penalty of employing switch transistors.

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