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Dual-clock MASH delta-sigma modulator employing a frequency modulated intermediate signal

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Abstract: A dual-clock MASH (multi-stage noise shaping) delta-sigma modulator (DSM) is proposed for high performance analog-digital converter. This employs a DSM using a frequency modulated intermediate signal (FMDSM) for the last stage. The sampling clock frequency for the last stage can be increased due to the features of the FMDSM. It is shown that this can increase the SNR beyond the conventional MASH DSMs.

Keywords: delta sigma modulator, analog digital converter, MASH
Classification: Integrated circuits

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1 Introduction

Among various types of analog-digital converters (ADCs) the delta-sigma ADC has a significant advantage that high resolution can be obtained without high-accuracy analog components, hence it is suitable for VLSI implementation [1]. However, its use is restricted to relatively low frequency applications due to the limitation of the sampling frequency. The DSM using frequency modulated intermediate signal (FMDSM) [2, 3, 4] has significant advantages that it has no feedback digital-analog converter (DAC) restricting the operation frequency, and hence, is suitable for high frequency operation. However, the FMDSM has been not widely used so far, since it is difficult to apply the FMDSM concept to higher order DSMs. In this paper we propose a novel configuration, the dual clock MASH (DCMASH), to construct higher order DSM using the FMDSM.

2 FMDSM

The configuration of the FMDSM is shown in Fig. 1 (a). This is based on the fact that the phase of the FM signal from the voltage-controlled oscillator (VCO), $\theta(t)$, is the integral of the input signal $x(t)$ as

$$\theta(t) = \int_{\tau=0}^{t} (2\pi f_c + kx(\tau))d\tau, \quad (1)$$

here, f_C represents the output frequency of the VCO when input is zero, and k the frequency sensitivity. Therefore the integrator in the conventional configuration can be removed. Moreover, the negative feedback is inherently embedded in the VCO, because the phase returns to zero when it reaches 2π. Owing to these features the feedback loop can be also removed. Using the 1-bit quantizer and the XOR the ideal pulse density signal can be obtained. This is suitable for high frequency operation, because it has no feedback DAC, which restricts the operation frequency of the conventional DSMs. However, it is difficult to construct higher order DSMs using this concept. This is because it needs difficult process, extracting the phase of the VCO output, which should be supplied to the second integrator. A circuit to extract phase was proposed in [5] assuming the rectangle waveform of the VCO output, but it is not suitable for high frequency operation. Another method is embedding the FMDSM into the inner part of the 2nd order DSM [3]. However, this has a global feedback loop for the outer DSM and the overall operation frequency should be restricted by it.

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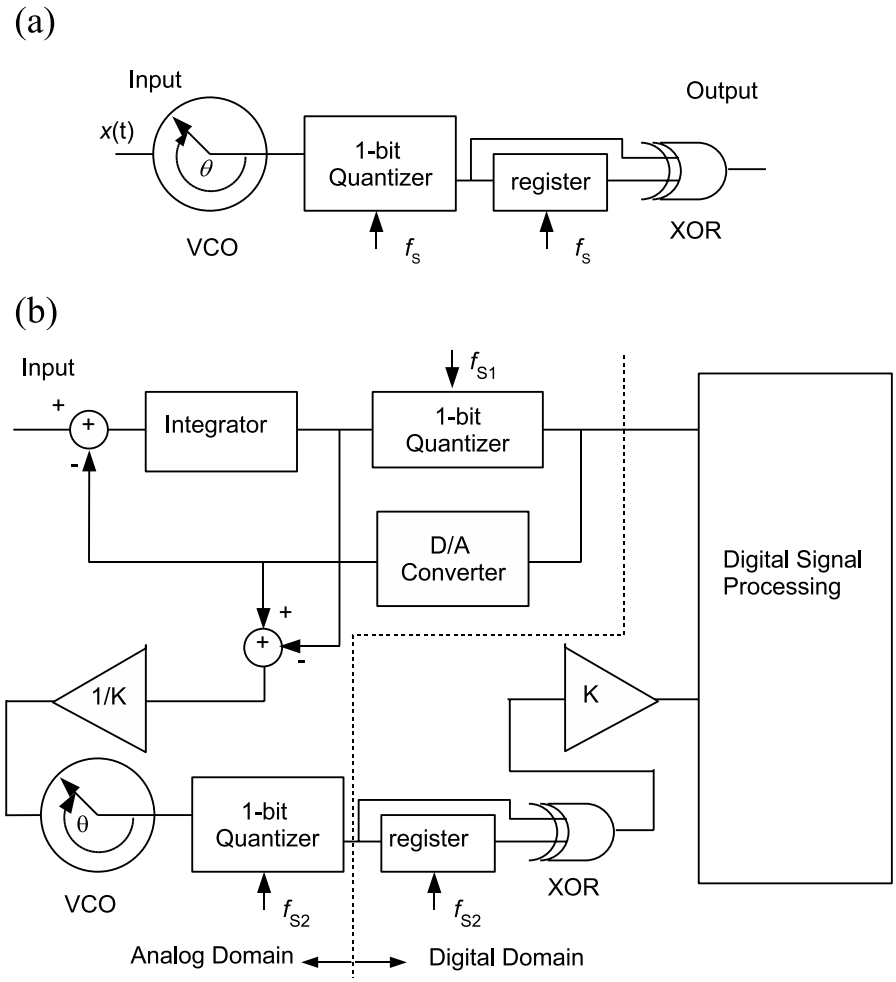

Fig. 1. Block diagram of the FMDSM (a) and DCMASH DSM (b).

3 Dual clock MASH DSM

Figure 1 (b) illustrates our proposal to apply FMDSM concept to higher order DSMs. In this configuration, the FMDSM is used for the second stage of the MASH (multi-stage noise shaping) DSM together with the continuous time DSM for the first stage. A key is that higher sampling frequency, f_{S2}, is used for the second stage than that of the first stage, f_{S1}. This is possible owing to the high speed nature of the FMDSM. The increase of the signal-to-noise-and-distortion ratio (SNDR) by the increase of f_{S2} can be expected as follows. The second stage DSM subtracts the first-order quantization noise from the first stage, and leaves the second order quantization noise sampled at f_{S2}. Thus, the frequency dependence of the quantization noise of this circuit should be 40 dB/dec just as the same as that of the conventional second order ones. This leads to the expectation that the SNDR increases with increasing f_{S2} by 50 dB/dec. However, the quantization noise signal from the first stage, which is sampled at lower-frequency, causes the overload in the second stage DSM. To avoid this one must attenuate the signal from the first stage by factor of $K = af_{S2}/f_{S1}$, where a is a number factor of the order of 1. Consequently, the maximum SNDR can be expressed as

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$$SNDR = SNDR_0(f_{S1}) + 30\log_{10}(f_{S2}/f_{S1}) - 20\log_{10} a. \quad (2)$$

Here, $SNDR_0(f_{S1})$ is the maximum SNDR for the conventional MASH DSM operating at f_{S1}. This indicates that higher SNR can be obtained beyond the conventional MASH DSM by increasing the clock frequency of the second stage DSM.

4 Simulation results

We have carried out simulations using Scilab [6] to demonstrate the DCMASH DSM. In this simulation, the components shown in the Fig. 1 (b) are assumed to be ideal. Figure 2 shows the obtained noise spectrum for the DCMASH, where the frequency is normalized by f_{S1}. The input was a sinusoidal signal at $f_{S1}/128$, and $f_{S2} = 32f_{S1}$, $a = 2$. The spectrum was calculated using Blackman-Harris window function. It is clearly shown that the noise decreases with decreasing frequency by 40 dB/dec. This is the same as the conventional second order DSM.

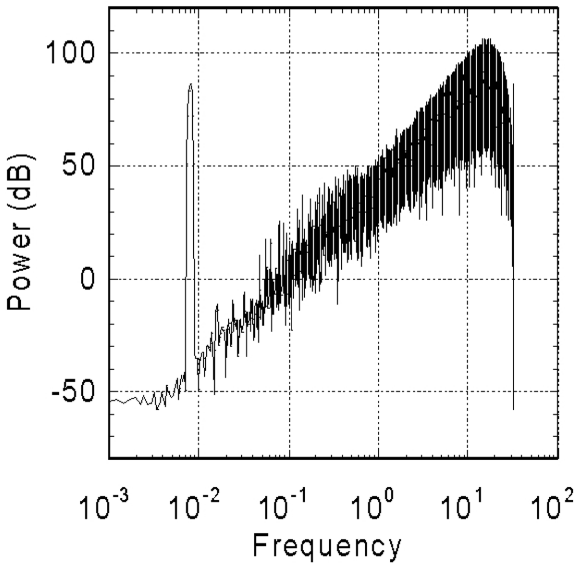

Fig. 2. Power spectrum for the DCMASH DSM. The frequency is normalized by f_{S1}. The input was a sinusoidal signal at $f_{S1}/128$, and $f_{S2} = 32f_{S1}$, $a = 2$.

Figure 3 shows the calculated SNDR as a function of the clock ratio f_{S2}/f_{S1}. The signal bandwidth was set to be $f_{S1}/64$. Two values 1 and 2 are used for a. When $a = 1$, overload occurs in the second stage. This decreases the total SNDR, so that the gradient of the SNDR reduces to 20 dB/dec. On the other hand, when $a = 2$, the SNDR increases with f_{S2} by 30 dB/dec, and agrees well with the Eq. (2). It should be noted that this method can be applied to higher order MASH, though we discuss only the second order MASH in this letter. Same increase of SNDR is expected for such higher order DCMASH by increasing the sampling clock for the last stage DSM.

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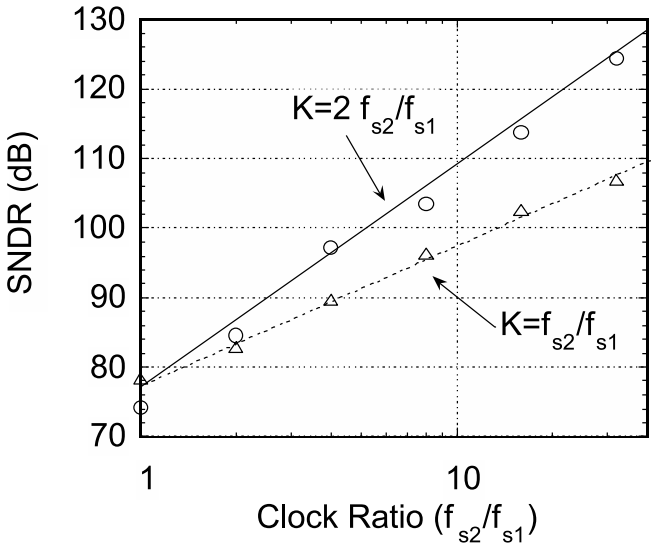

Fig. 3. Calculated SNDR for the DCMASH DSM as a function of the frequency ratio f_{S2}/f_{S1}. The input was a sinusoidal signal at $f_{S1}/128$, and the signal bandwidth was $f_{S1}/64$. Open circles and triangle are for $a = 2$ ($K = 2f_{S2}/f_{S1}$) and $a = 1$ ($K = f_{S2}/f_{S1}$), respectively.

Finally, we mention about the severe requirement for the VCO, and how to overcome it. The VCO must have high linearity and wide range of frequency modulation for fully exploiting the dual-clock MASH technique. Recently, we have proposed a novel circuit to realize such VCOs, which is based on the down-conversion of high frequency signals [7]. Furthermore, FMDSM has a significant advantage that it is easy to implement multi-bit DSM employing parallel DFFs [8]. With these techniques the difficulties in designing the VCO should be much reduced. Consequently, the dual-clock MASH DSM using FMDSM is promising for high-resolution, wide-band ADCs.

5 Conclusion

A dual-clock MASH DSM was proposed employing the FMDSM for the last stage. Owing to the FMDSM's ability for high frequency operation, the sampling clock frequency of the last stage modulator can be increased beyond the other stages. It is demonstrated that increasing the last stage sampling frequency increases the SNDR by 30 dB/dec beyond the conventional MASH DSMs.

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