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A low-voltage PWM CMOS imager with small pixel size using an in-pixel gate-common comparator

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Abstract: We propose a new pixel structure of pulse-width-modulation (PWM) CMOS active pixel sensor with a small pixel size performing a pixel-level single-slope A/D conversion to realize a low and single power supply operation. The pixel is composed of only three transistors without pixel-circuit sharing, and has a gate-common amplifier that compares a photodiode voltage on the gate node with a ramp signal on the source for A/D conversion. We have fabricated a 128×96-pixel prototype imager with an on-chip ramp generator and bootstrap circuits in a 0.35-μm CMOS technology, and successfully demonstrated image acquisition with a 1.4-1.8-V single power supply.

Keywords: CMOS imager, pulse width modulation, low voltage

Classification: Integrated circuits

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1 Introduction

Low voltage operation of pixels, analog front-ends, and A/D converters of CMOS imagers [1] is a challenge to realize a low voltage and single power supply CMOS imager that can be merged with various digital circuits in a system on a chip. To operate the analog parts of the CMOS imagers at low voltage without degrading the sensor performances, pulse modulation pixel readout schemes [2, 3], especially a pulse-width-modulation (PWM) scheme [4, 5, 6, 7] is suitable. In the PWM scheme, the pixel value is represented by the width of a digital pulse, and such a temporal coding scheme enables us to lower the power supply voltage with less dynamic range degradation [7]. The pulse width can be easily converted to a digital value by counting it with a counter and latch memories [8], which is called a single-slope A/D conversion. In spite of the above advantages, the PWM-based CMOS imagers have a significant issue concerning a large pixel size or a small fill factor because they have in-pixel comparators composed of several transistors [5] or with a capacitor [4, 7]. Therefore, PWM CMOS imagers are not necessarily suitable for consumer or low-cost applications.

In this paper, we propose a new small-sized pixel structure based on a PWM pixel readout scheme. The number of transistors in a pixel is only three without any circuit sharing technique between several pixels, which is same as that of the ordinary 3T active pixel sensor (APS). A prototype imager is fabricated in 0.35-μm CMOS technology, and image acquisition is demonstrated.

2 PWM CMOS imager with in-pixel gate-common comparators

Figure 1 (a) shows a simplified schematic of the proposed PWM CMOS imager. A timing generator and bias circuits are off-chip in this prototype. We propose to utilize a gate-common amplifier as an in-pixel comparator. With our scheme, the number of the transistors of the in-pixel comparator is only one, which offers the smallest pixel to our knowledge comparing with the existing PWM CMOS imagers. With a larger gain of the gate-common transistor than those of the source followers used in pixel readout of the ordinary CMOS imagers, the benefits of the PWM readout scheme such as low voltage operation and pixel-level A/D conversion are available. The pixel is composed of a photodiode (PD), a reset transistor (M_{RST}) for feedback reset of the PD, a select transistor (M_{SEL}), and a gate-common-amplifier tran-

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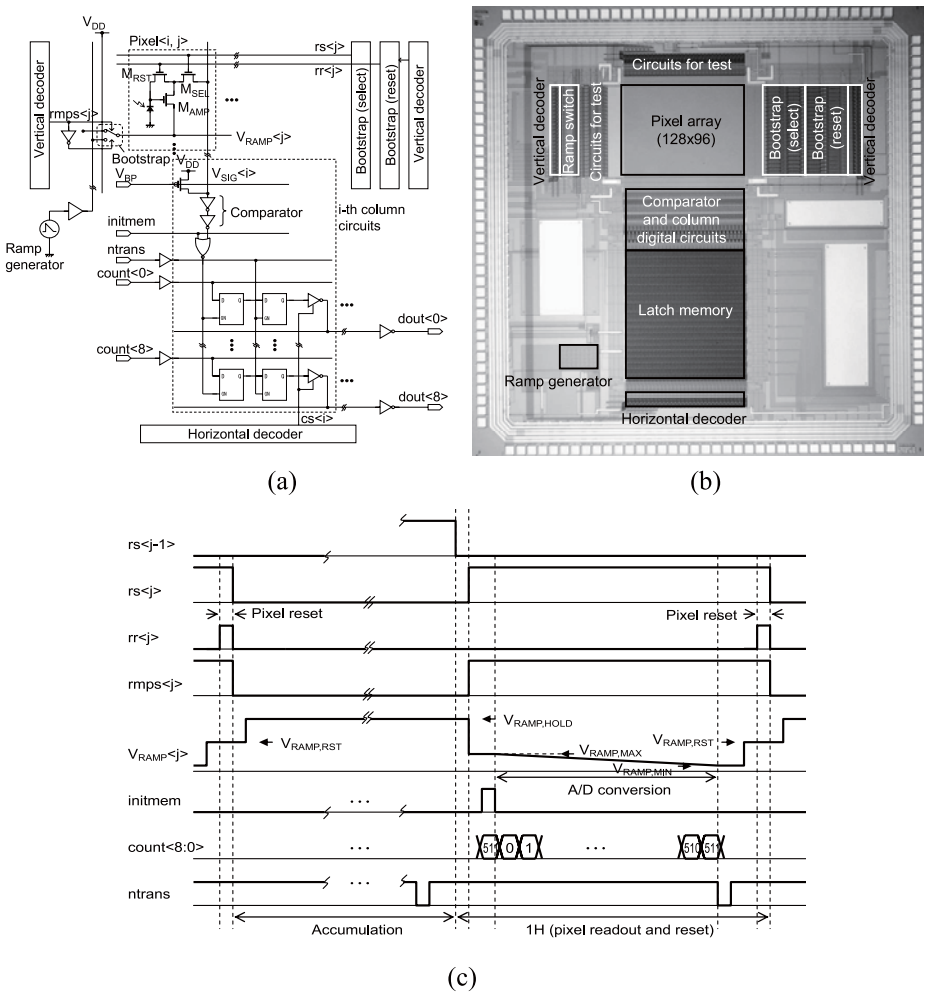

Fig. 1. (a) Simplified schematic of PWM CMOS imager, (b) microphotography of the fabricated CMOS imager, and (c) timing chart.

sistor (M_{AMP}) working as a comparator. Neither depletion transistor nor low-threshold-voltage transistor is used. The PD is embodied by a simple P-substrate/ N-well junction. In pixel readout, a ramp signal is applied to the source node of M_{AMP}. The threshold voltage of the gate-common amplifier is modulated by the photodiode voltage, so that the timing when the comparator output (in other words, the pulse width) changes depends on the illumination.

Figure 1(c) shows a timing chart of pixel readout and reset. At the end of the pixel readout, the pixels in the j-th row are reset. In resetting, rs<j> and rr<j> are high at the same time, which are bootstrapped to the voltage higher than the power supply voltage (V_{DD}) to let M_{SEL} and M_{RST} completely turn on. rmps<j> is also high to supply a reset voltage, $V_{RAMP,RST}$<j>, from a ramp generator [9] to the source node of M_{AMP}. In resetting, M_{AMP} works as a source-common amplifier. Photodiode voltage, V_{PD}, is reset to $V_{RAMP,RST}$<j>+V_{TH} + ΔV_{TH} approximately. Note

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that V_{TH} and ΔV_{TH} are the threshold voltage and its variation of M_{AMP}, respectively. After pixel reset, $V_{RAMP}<j>$ becomes $V_{RAMP,HOLD}$ around V_{DD} to make M_{AMP} completely turn off to suppress the sub-threshold leak current. After the accumulation period, a pixel readout period begins. A ramp-shaped voltage signal is applied to the source node of M_{AMP} and it is compared with V_{PD}. In cooperation with a column comparator and a counter memory, semi-pixel-level ADC is executed. Because the gain of the in-pixel comparator is not large enough to completely binarize the pixel value, the column comparator is used. Firstly, rs<j> and rmps<j> become a boot-strapped high level, and $V_{RAMP}<j>$ is set to the start voltage of the ramp signal, $V_{RAMP,MAX}$. The column memory is reset to the maximum value (=511 for ADC resolution of 9-bit) by activating signal initmem. The ramp signal, $V_{RAMP}<j>$, begins to decrease at a constant rate down to the minimum voltage, $V_{RAMP,MIN}$. We denote $V_{RAMP,MAX}$ -$V_{RAMP,MIN}$ by ΔV_{RAMP} that defines the saturation and the sensitivity of the pixel readout. According to the ramp voltage, the digital count value, count$<8:0>$, increases from 0 to 511, and is applied to the memory block. When we denote the change of V_{PD} during the accumulation period by ΔV_{PD}, M_{AMP} turns on when $V_{RAMP}<j>+V_{TH}+\Delta V_{TH} = V_{RAMP,RST}<j>+V_{TH}+\Delta V_{TH}$-$\Delta V_{PD}$, namely, $V_{RAMP}<j>= V_{RAMP,RST}<j>$-$\Delta V_{PD}$. This means that ΔV_{TH} is cancelled if the slew rate of the gate-common comparator is larger than that of the ramp signal multiplied by the gain of the comparator. If M_{AMP} turns on, the voltage of the vertical signal line, $V_{SIG}<i>$, begins to decrease quickly. When $V_{SIG}<i>$ becomes smaller than the threshold voltage of the column comparator, its output turns to low, and the count value just before the output change, which is the ADC result of the pixel value, is held by the latch memories. After the ADC, the contents of the latch memories are transferred to those for off-chip readout.

In the circuit design, we have to care the resistance of the horizontal ramp signal line to suppress its voltage fluctuation. When R_{PIX}, I_{PEAK}, and N_X denote the resistance of the ramp signal line, the peak current introduce by M_{AMP}, and the number of horizontal pixels, respectively, the maximum voltage fluctuation give by $(1/2)N_X(N_X\text{-}1)R_{PIX}I_{PEAK}$ should be smaller than 1/2-LSB of the ADC.

3 Experiments

Figure 1 (b) shows the microphotograph of the prototype imager fabricated in a 0.35-μm standard CMOS technology. The specifications of the imager are shown in Table I. Compared with a pixel in Ref. [7] fabricated in the same generation technology, the pixel is shrunk to 44% in area. Although the fill factor is limited to 18.5% with a standard fabrication technology, it will be improved to be more than doubled with CMOS imager technologies. To demonstrate the operation of the proposed pixel structure, we have executed image acquisition and measured the characteristics. In the experiment, a frame rate was 5.5 fps, and power supply voltages ranged from 1.1 V to 1.8 V.

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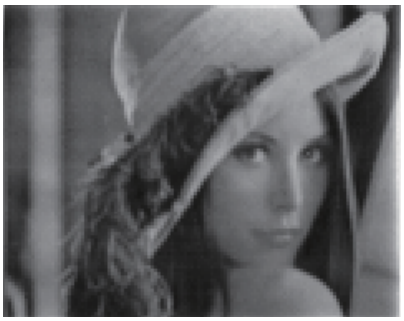

Fig. 2. An example of the captured image with digital CDS. V_{DD} and ΔV_{RAMP} were 1.5 V and 0.4 V, respectively. A white defect pixel was filled with a neighboring pixel value.

Table I. Specifications and characteristics of the PWM CMOS imager.

Technology	0.35-μm CMOS (2-poloy, 3-metal, no photodiode option)
Pixel size	10 μm sq.
Pixel counts	128 x 96
Fill factor	18.5%
Power supply voltage	1.4-1.8 V
Frame rate	5.5 fps
Dynamic range	48.8 dB@V_{DD}=1.5 V, ΔV_{RAMP}=0.4 V
Column FPN (rms)	0.7% (without CDS), 0.033%(with digital CDS) @V_{DD}=1.5 V, ΔV_{RAMP}=0.4 V
Power dissipation	72.8 μW (total) @ V_{DD}=1.4 V, ΔV_{RAMP}=0.2 V 21.3 μW (pixel array) 51.5 μW (column comparator, and digital circuits) 0.042 μW (ramp generator)

Digital correlation double sampling (CDS) was executed in pixel readout to reduce fixed pattern noises (FPNs). Although the ADC operations and off-chip readouts of the results of ADC could be executed simultaneously, they were separated to avoid the additional noises. Figure 2 shows an example of the captured image with the digital CDS technique when V_{DD} and ΔV_{RAMP} were 1.5 V and 0.4 V, respectively. Column FPNs were reduced by about 1/20 with the digital CDS. The lowest power supply voltage with single analog and digital power supply was 1.4 V. The pixel readout circuits could operate even at 1.2 V. However, the digital circuits of the prototype malfunctioned below 1.4 V. Improvement of the digital design or application of a more advanced fabrication technology will enable us to lower the power supply voltage further. Power dissipation in dark with 1.4-V power supply was shown in Table I. Large power dissipation of the column comparators was caused by the transition current of the CMOS inverters due to small slew rate of the ramp signal. This problem can be alleviated by increasing the frame rate in the future design or changing the circuit architecture of the column comparators.

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4 Conclusion

We have proposed the smallest PWM pixel structure without any pixel sharing technique, and successfully demonstrated the operations of the 128×96-pixel prototype PWM imager fabricated in a 0.35-μm CMOS technology with 1.4-1.8 V single power supply voltages. The imager is based on a PWM readout scheme employed with a gate-common amplifier as a one-transistor in-pixel comparator. The number of transistor in a pixel is three, which is as many as that of ordinary 3T APS. FPNs caused by variation of threshold voltages and gains of the amplifier transistors were successfully reduced with a digital CDS technique.

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