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Low power high performance level converter for dual supply voltage systems

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Abstract: A low power high performance level converter circuit is presented. The performance and the robustness of this level converter are compared to those of the previous level converters using HSPICE simulations in a 65 nm standard CMOS technology. The results of the comparison with the previously proposed circuits show 63%, 33%, 35%, and 8% reduction in the average power, the static power, the delay, and the area, respectively.

Keywords: low power, high performance, level converter

Classification: Integrated circuits

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http://www.device.eecs.berkeley.edu/˜ptm.

1 Introduction

The power dissipation of digital circuits has become a very important design parameter in recent VLSI designs [1]. Some of the reasons for this importance include the limited battery lifetime used in portable devices such as cell phones and laptops and the limit on the maximum temperature of the chip. The power consumption of a digital circuit includes dynamic, short circuit, and static (leakage) power consumption. Several techniques have been proposed for reducing the power consumption. One of the effective approaches to reduce the power consumption is to scale the supply voltage. This technique reduces all the components of the power consumption. Reducing the supply voltage, however, leads to the speed degradation unless the supply voltage of the design critical path(s) becomes higher compared to the supply voltage of other parts of the circuit (see, e.g., [2]). This leads to two supply voltages for the circuit. Another approach to prevent the speed degradation when using lower supply voltage is to use transistors with a smaller threshold voltage in the critical path (see, e.g., [2]).

Using these two techniques, the speed of the critical path is not degraded while the power dissipation of the circuit is reduced [3]. The problem with dual supply voltage systems is that when a block with low supply voltage ($VDDL$) is connected to a block with high supply voltage ($VDDH$), the static current of the latter block increases. This is shown in Fig. 1 (a) where an inverter with $VDDL$ is connected to an inverter with $VDDH$. As observed from the figure, when the output of the first inverter is high, the source-gate voltage of the PMOS transistor is greater than zero giving rise to a significant

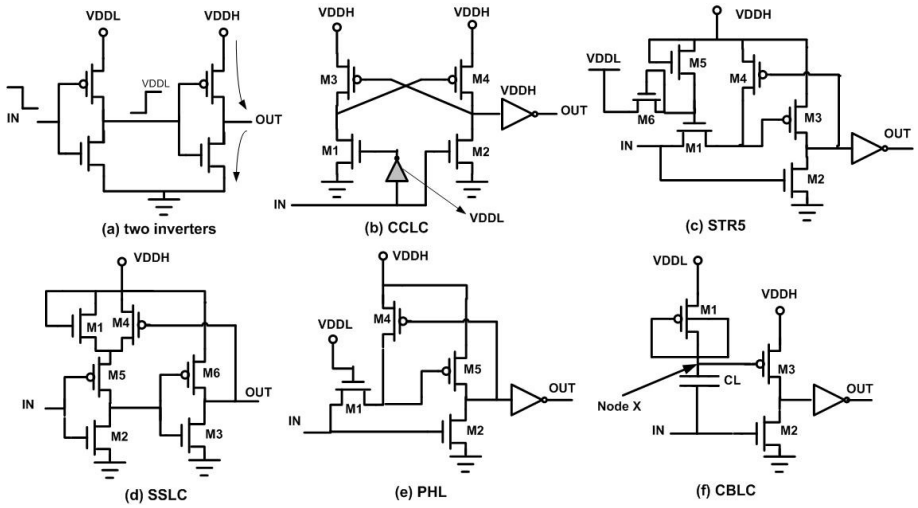

Fig. 1. The circuit structure of two connected inverter with dual supply voltage, existing and proposed level converters.

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increase in the static current. To overcome this problem, level converter circuits, which convert *VDDL* to *VDDH*, should be used at the boundary of the two blocks. Several level converter circuits have been proposed in the literature (see, e.g., [2, 4, 5, 6]). Cross-coupled PMOS pair (CCLC) [2], STR5 [4], single-supply diode-voltage limited buffer (SSLC) [5], and pass transistor half latch [6] are among the level converter circuits suggested in the literature to provide an effective solution for dual supply systems [6]. The level converter circuits, however, impose some power, delay, and area overheads. In this work, we have focused on reducing the overheads.

2 Previous level converter

The cross-coupled PMOS pair level converter (CCLC) is shown in Fig. 1 (b) [3]. When the input is low, the output of the VDDL inverter becomes high turning on the NMOS transistor M1. This discharges the node X turning on the PMOS transistor M4. This charges the drain of M1. After a delay equal to the delay of the VDDH inverter, the output of the circuit becomes low. The speed of this level converter which has been widely used is very low [3]. In addition, this converter has some layout placement limitations [3]. The latter problems originate from the dual supply voltage requirements of the converter. Another level converter, which is shown in Fig. 1 (c), has more transistors and area is STR5 [4]. As seen from this figure, M4 is a feedback device which prevents the short circuit current from flowing trough the inverter while M5 acts as a pull-up device. M6 is added to prevent the gate voltage of M1 transistor from rising above $VDDL + Vth$ which can lead to the leakage current through M1 [4]. Also, in the steady state, the leakage current can flow through M5 and M6 from *VDDH* to *VDDL*. Therefore, the leakage power in this level converter is high. In order to eliminate the layout placement limitations of the level converter, the single-supply diode-voltage- limited buffer (SSLC) which makes use of one supply voltage has been proposed in [5]. In Fig. 1 (d), the circuit of the SSLC is shown. In this circuit, the voltage drop across the diode connected NMOS transistor M1 provides the NMOS transistor M2 and the PMOS transistor M5 with a low supply voltage. In addition, due to the shorter distance from the input to the output, this level converter is faster than the CCLC. Another level converter which is called pass-transistor half latch (PHL) is shown in Fig. 1 (e) [6]. This level converter also employs the dual supply rail and, hence, it has more complex routing than that of the SSLC.

3 Proposed level converter

As mentioned previously, the use of the dual supply voltage technique without using level converters leads to a weak turn-off of the PMOS transistor and, hence, a significant increases in the static current. In the circuits discussed in the previous section, only transistors were used in the converters. In this paper, we propose a capacitive based level converter (CBLC) which is based on a capacitance charging effect. The circuit diagram of the converter

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which consists of a capacitor and five transistors is shown in Fig. 1 (f). The converter makes use of the charge stored in the capacitor to guarantees the proper operation of the device for each input signal. After some delay, the capacitor charge reaches its steady state value which is the low supply voltage (*VDDL*). The waveforms for the input voltage and the voltage of the node X in the steady state are plotted in Fig. 2 (a). As observed from this figure, when the input signal is low, the diode-connected transistor turns on and the capacitor *CL* can be re-charged to *VDDL* for any possible discharge. For this transistor, the body is connected to the node X causing the bulk-source junction to become forward-biased. This injects additional charging current from the bulk of the transistor M1 to the node X. When the input is low, M3 becomes on and the output reaches its final value that is low. Thus, the input voltage passing through two inverters makes the output to be low as it should be. When the input rises to *VDDL*, the PMOS transistor M1 turns off forcing the node X to be float. The gate voltage of M3 becomes 2*VDDL* which is the sum of the input voltage and the capacitor voltage. In this case, the output voltage becomes high as it is desired. In the steady state, the voltage of node X is equal or higher than *VDDL*. When it is higher than *VDDL*, the terminal connected to the node X behaves as the source for M1. In this case, the transistor source and bulk become connected to each other.

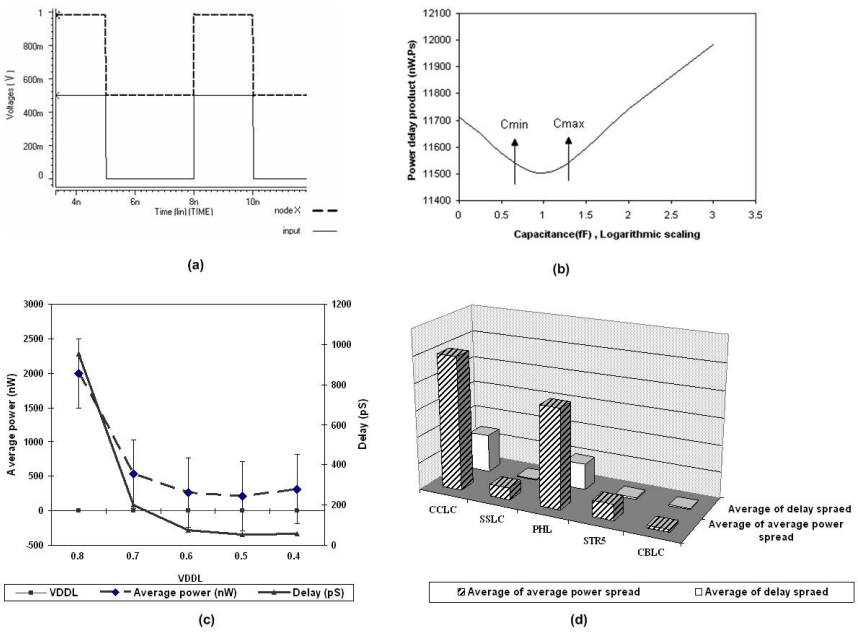

Fig. 2. (a) The voltage of the node X (dashed line) and the input voltage (solid line) waveforms. (b) Power delay product CBLC versus the size of the capacitance in logarithmic scaling. (c) Average power and delay in CBLC level converter versus *VDDL*. (d) Comparison of average of average power and delay spread by ±10% bouncing in each of two power supplies in CCLC, SSLC, PHL, STR5, and CBLC level converters.

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4 Results and Discussion

The level converters discussed here include CCLC, SSLC, PHL, STR5, and CBLC. To measure the average dynamic power, we have applied random inputs to each structure and measured the average power during the period that input is applied. The delay is obtained by averaging the rising and falling propagation delays. To measure the static power, we have assumed the applied input is zero and the circuit is in the steady state condition. The length of all transistors and the width of each transistor located in the non-critical path are set to the minimum length (65 nm). The widths of the transistors located on the critical path are determined to have a minimum power delay product. Similar to [7], the input noise margin in this paper is defined as the input voltage that causes 10% voltage drop at the level converter output. The sizings of the transistors in the CBLC and other level converters have been determined by optimizing the power delay product. This sizing approach, however, affects the noise margin. For instance, although using a wider M3 improves the noise margin but it also increases the power due to the larger flowing current through M3. If the noise margin is a prime concern in a design, then the sizing approach should be based on minimizing this parameter. In this work, with the sizing approach of minimizing the power delay product, the input noise margin is set to be 20% of $VDDH$. The results of the HSPICE simulations for these converters are given in Table I. The circuits were implemented in a 65 nm standard CMOS technology [8] with $VDDL = 0.5$ V, $VDDH = 1$ V, the clock frequency of 200 MHz and the load capacitance (CL) of 10 fF. As seen from this table, the delay, the average dynamic power (average power), the static power, and the area of the proposed level converter are lower than the same parameters of the previous level converters. To calculate the area, we have added up the transistor widths of the circuits. Also, to calculate the improvement, we have used the best parameter of the previous converters.

Table I. Comparison of level converters' performance and level converters' robustness.

	CCLC	SSLC	PHL	STR5	CBLC
Average Power (nW)	2790	364	2225	632	213
Average power spread for ±10% bounce in VDDH (nW) (VDDL = 0.5V)	1854	306	1671	414	88
Average power spread for ±10% bounce in VDDL (nW) (VDDH = 1V)	3170	148	2048	198	20
Average of the average power spread for ±10% bounce in VDDL and VDDH (nW)	2512	227	1860	306	54
Delay (pS)	655	78	503	78	54
Delay spread for ±10% bounce in VDDH (pS) (VDDL = 0.5V)	243	22	210	10	34
Delay spread for ±10% bounce in VDDL (pS) (VDDH = 1V)	1198	30	773	50	7
Static Power (nw)	6.8	6.2	6.1	42	4.1
Area (nm)	555	390	390	520	360
Improvement of CBLC in comparison with the best one					
Average Power (nW): 63%	Delay (pS): 35%				
Static Power (nw): 33%	Area (nm): 8%				

To show the effect of the capacitance size on the converter parameters, we

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have plotted the power delay product of CBLC as a function of capacitance *CL* in Fig. 2 (b). As observed in this figure, when the capacity of *CL* becomes less than some *CMIN*, the power delay product will increase. This is caused by a more static power induced by the current flowing through M3 and M2. In this case, the capacitance (*CL*) cannot charge completely and, hence, its voltage cannot reach to the desirable value (*VDDH*) in the given time determined by the circuit frequency. In addition, the charge sharing effect can decrease the voltage drop on it. On the other hand, when the capacitance of *CL* is more than *CMAX*, the power delay product will increase, too. This is caused by the fact that the dynamic power and the delay will increase when the capacitance increases. As seen from this figure, choosing capacitance of *CL* about 10 fF which has the minimum power delay product can be a good choice. Besides these factors, the charge sharing effect plays a major role in the variation of the power consumption and also in the power delay product when *CL* is more than *CMAX* and less than *CMIN*.

The design of dual-supply level converter should be done carefully to minimize the bounce on both *VDDL* and *VDDH* rails. In other words, being more sensitive to the bouncing on these supplies makes the level converter being less robust [6]. In order to examine the sensibility of the CBLC converter to bouncing on supply voltages, we have measured its delay and average power while two supply voltages have been changed. The delay and average power values of proposed level converter as shown in Fig. 2 (c) are minimized when *VDDL* becomes 0.5 V. Therefore, we compare this level converter with the previous ones by changing *VDDL* around this point. Table I shows the simulation results for the delay and the average power values for CCLC, SSLC, PHL, STR5, and CBLC when *VDDL* has a bouncing of ±10% and *VDDH* is constant (1 V) and when *VDDH* has a bouncing of ±10% and *VDDL* is constant (0.5 V). Also, the average values for the delay and the average power spread in these level converters considering the ±10% bouncing on *VDDL* and *VDDH* are shown in Fig. 2 (d). The low sensibility of the CBLC level converter to the supply bouncing shows its higher robustness.

5 Conclusion

In this paper, we proposed a high performance yet low power level converter circuit. The circuit made use of a capacitor to lower the power and the area. The HSPICE simulation results for a 65 nm standard CMOS technology showed 35%, 63%, 33%, and 8% reductions in the delay, the average power consumption, the static power, and the area, respectively when compared to those of the previous level converters. The simulation results also showed that a high robustness of the proposed level converter beside its higher performance.

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