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A fast programmable frequency divider with a wide dividing-ratio range and 50% duty-cycle

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Abstract: A novel programmable frequency divider in 0.18-μm standard CMOS process is presented in this paper. With less cascode CMOS-stages, the proposed design achieves a higher operating frequency compared to that of the similar programmable frequency dividers reported in the literature. Test results demonstrate that the divider can operate up to 4.5 GHz. Elimination of passive resistors in the proposed scheme provides an area efficient design approach. Design improvements to achieve 50% duty cycle are also presented. Due to the lower operating frequency of the 50% duty cycle correction unit, it only adds a very small amount of power consumption penalty ($\sim$ 10%) to the entire system.

Keywords: programmable frequency divider, ring VCO, D latch, 50% duty-cycle

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Recently high performance programmable dividers are getting more and more concerns in RF integrated circuit design field for efficient and reliable operation of the entire system. It is an important portion of a frequency synthesizer. Programmable dividers are also widely used to generate variable clock-signals for: switched-capacitor filters (SCFs), digital systems with different power-states, as well as multiple clock-signals on the same SOC (system-on-a-chip). A programmable divider can divide an input frequency by a desired programmable ratio. High operating frequencies, wide divide-ratio ranges, binary divide-ratio controls and 50% duty-cycle are the most common features of a highly efficient programmable frequency divider. A number of programmable dividers have been reported in the recent years [1, 2, 3, 4, 5], but none of them meet all the desired characteristics.

Vaucher *et al.* designed a programmable frequency divider with a wide dividing-ratio range of 8 $\sim$ 524287 [1]. This paper presents a modified programmable frequency divider following the work reported in [1]. In order to achieve higher operating frequencies, the proposed design reduced the number of cascode CMOS stages. The divider circuit has been fabricated using 0.18-μm standard CMOS process. The test results verify that the divider can operate at high frequencies up to 4.5 GHz.

The circuit in [1] also has a disadvantage that its output pulse width is only 2 or 3 times of the input period. If the input frequency is 2 GHz, the output pulse width is only 1ns or 1.5 ns. The output pulse width does not change if the output frequency is lower. It is therefore very difficult to drive big clocked systems using these narrow pulses. The divider may not be able to charge the load capacitors to the correct logic level of the clock signal. If the duty-cycle is close to 50%, the output pulse width will be much longer. With the same current at the output stage, the driving capability of the divider will be greatly increased. A method to make the output duty-cycle of the programmable divider very close to 50% is presented. Test results corroborate the efficacy of the design.

2 Proposed Programmable Divider

2.1 Circuit schematics

A programmable frequency divider can have a wide range of dividing ratios ($2^{\min} \sim 2^{\max+1} - 1$) [1]. The designer can specify the minimum power value 'min' and the maximum power value 'max'. The binary control-digits (P_0, P_1, ..., P_n) are used to set the dividing ratios. The block diagram of Vaucher's divider is shown in Fig. 1 (a) ('Div_n_vaucher'). The proposed design has modified internal building blocks of 'Div_n_vaucher' for higher frequency operation and reduced layout area. Each proposed block consists of a

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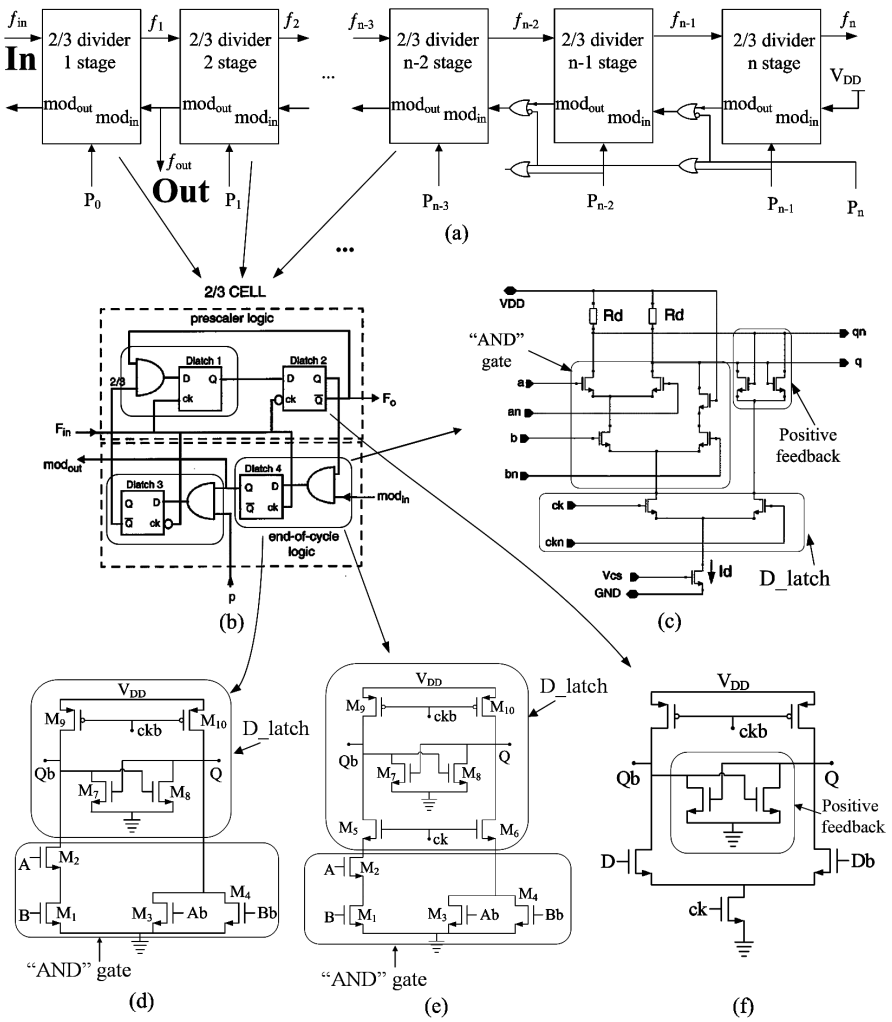

Fig. 1. (a) Schematic of Vaucher's divider ('Div_n_vaucher') shown in [1] (b) Schematic of the 2/3-divider cell shown in [1] (c) The original combined AND-latch shown in [1] (d) The proposed combined AND-latch for the 1st 2/3-divider stage (e) The proposed combined AND-latch for the 2nd to the last 2/3-divider stages (f) The proposed D_latch in the 2/3-divider

divide by 2 or 3-divider. The first 2/3-divider block needs to be operated at the input frequency, while the subsequent blocks will be operated at reduced frequencies.

Through derivations, the dividing ratio of Vaucher's divider is obtained:

(1a) *If all of* $P_{\min+1}, P_{\min+2}, \ldots, P_{\max-1}, P_{\max} = 0$, *or division ratio* $< 2^{\min+1}$

$$\begin{aligned} \textit{division ratio} &= P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min-1} \cdot 2^{\min-1} + 2^{\min} \\ &= \sum_{i=0}^{\min-1} P_i \cdot 2^i + 2^{\min}; \end{aligned} \tag{1}$$

(1b) *Otherwise* (*If any of* $P_{\min+1}, P_{\min+2}, \ldots, P_{\max-1}, P_{\max} = 1$), *or division ratio* $\geq 2^{\min+1}$

$$\textit{division ratio} = P_0 \cdot 2^0 + P_1 \cdot 2^1 + \cdots + P_{\min-1} \cdot 2^{\min-1} + P_{\min} \cdot 2^{\min} + \cdots$$

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$$+P_{\max-1}\cdot 2^{\max-1}+P_{\max}\cdot 2^{\max} = \sum_{i=0}^{\max} P_i\cdot 2^i$$

If the dividing ratio is $< 2^{\min+1}$, set P_{min} to logic '1', since $P_{min+1}, \ldots, P_{max} = 0$, Eq. (1b) can express the dividing ratio in Eq. (1a). Thus Eq. (22) alone can be used to express the dividing ratio for all cases.

When the dividing ratio $< 2^{\min+1}$, set P_{min} to logic '1', then

$$\textit{divide ratio} = P_0\cdot 2^0+P_1\cdot 2^1+\cdots+P_{\min}\cdot 2^{\min}+\cdots +P_{\max-1}\cdot 2^{\max-1}+P_{\max}\cdot 2^{\max} \quad (2)$$

For the 'Div_n_vaucher' circuit shown in Fig. 1 (a), min = n − 2, and max = n. If the dividing ratio is $< 2^{n-1}$, set P_{n-2} to logic '1', the dividing-ratio for Fig. 1 (a) will be:

$$\textit{dividing ratio} = P_0+P_1\cdot 2^1+P_2\cdot 2^2+\cdots+P_{n-1}\cdot 2^{n-1}+P_n\cdot 2^n \quad (3)$$

In order to operate at higher frequencies, a few changes are made in Vaucher's 2/3-divider cell, as shown in Fig. 1 (b). There are three combined 'AND-latch' and one 'D_latch'. The circuit in Fig. 1 (c) shows Vaucher's 'AND-latch' design, a combination of an 'AND' gate and a 'D_latch'. Fig. 1 (d) shows the proposed 'AND-latch' design for the 1st 2/3-divider stage whereas Fig. 1 (e) depicts the 2/3-divider stages for the 2nd to the end. Fig. 1 (f) shows the proposed 'D_latch' circuit used in each 2/3-divider block.

In Fig. 1 (c), the 'D_latch' part is used to allow the outputs to change when the clock signal 'ck' is high. The 'positive feedback' is used to hold the outputs 'q' and 'qn' when 'ck' is low. The proposed 'AND-latch' designs are shown in Fig. 1 (d) and 1 (e), whose difference is stated as the following. The gates of M_5 and M_6 in Fig. 1 (e) are connected to the clock signal 'ck'. In Fig. 1 (d), M_5 and M_6 are removed, enabling the circuit to yield faster operation. Compared to the Vaucher's design, the proposed design has higher operating frequency due to less cascode-transistor stages, and much less layout area due to the elimination of the passive resistors.

2.2 Test Results

The programmable frequency divider is fabricated using TSMC 0.18-μm standard CMOS process. An on-chip VCO (Voltage Controlled Oscillator) generates high input frequency signals for the frequency divider. The proposed frequency divider can operate up to 4.5 GHz with a 3 V power supply.

The programmable frequency divider is tested using an Agilent E4407B spectrum analyzer. The output spectra are shown in Fig. 2. The input frequency can be calculated as $f_{out}\times$ dividing-ratio. For both of the Fig. 2 (a) and (b), the ring VCO has an output frequency of about 4.46 GHz. As the dividing ratio was varied between 66 and 71, the output frequency of the programmable frequency divider ('Mkr1 ***MHz', shown in the top right part of the figures) changed correspondingly.

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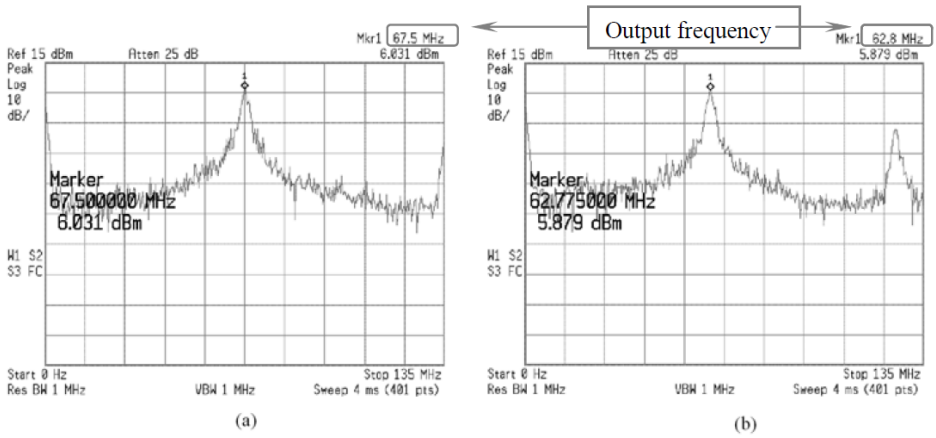

Fig. 2. Test results of output spectra. f_{in} is 4.46 GHz, VDD = 3 V (a) The dividing ratio is 66, and f_{out} = 67.5 MHz, (b) The dividing ratio is 71, and f_{out} = 62.8 MHz

2.3 Design Improvement to obtain 50% output duty-cycle

The output pulse width of Vaucher's design is very narrow. Thus Vaucher's divider has poor capability to drive other circuits. The circuit in Fig. 3 can generate an output with very close to 50% duty-cycle, while retaining the same dividing ratios as 2^{min} to $2^{max+1} - 1$.

To get 50% duty-cycle, a divide-by-2 divider, 'Div2', is added at the output of 'Div_n_vaucher' (shown in Fig. 1 (a)). An 'AND' gate and an 'n bit half adder' are also included in the feedback loop as shown in Fig. 3. The original output signal is 'f_{out_origin}' (top-middle part), whose duty cycle is far-off 50%. The duty cycle of the proposed output, 'f_{out}' (top-right part), is very close to 50%. This is because 'f_{out}' is the output of 'Div2', and the period of 'f_{out_origin}' changes very little. S_0, S_1, ..., S_n are the dividing-ratio controls of the proposed divider. 'S_0' is the LSB (Least Significant Bit). 'f_{out}'

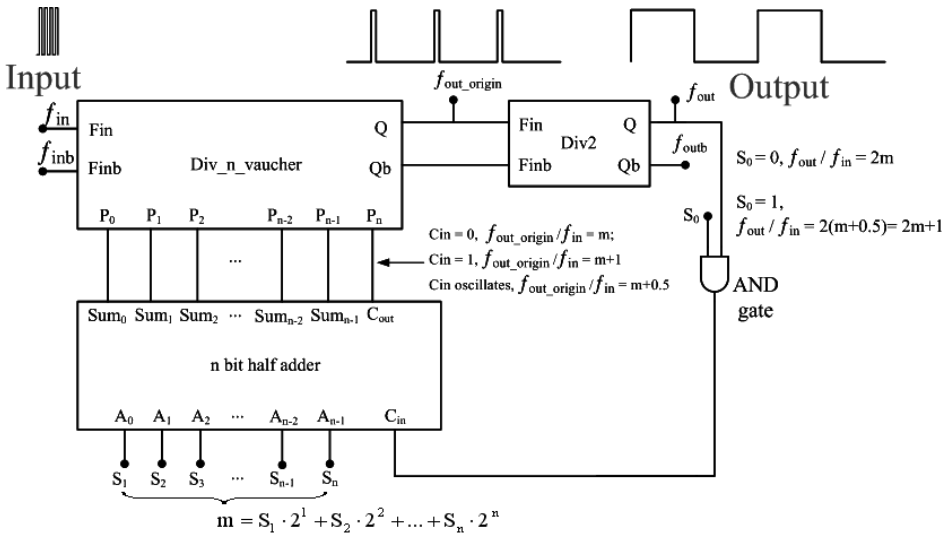

Fig. 3. Schematic of the proposed design with 50% output duty-cycle

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and 'S_0' are the inputs of the 'AND' gate. The output of the 'AND' gate is fed to the C_{in} input of the 'n bit half-adder'. The outputs of the adder are used as the dividing-ratio controls for the 'Div_n_vaucher'.

Use 'm' to represent the binary combination of (S_1, S_2, ..., S_n), so $m = S_1 + S_2 \cdot 2^1 + S_3 \cdot 2^2 + \cdots + S_{n-1} \cdot 2^{n-2} + S_n \cdot 2^{n-1}$. For the 'Div_n_vaucher' in Fig. 1 (a), $P_{min} = P_{n-2}$, and $P_{max} = P_n$ as stated in section 2.1. If the dividing ratio of the 'Div_n_vaucher' is $< 2^{n-1}$ (or the proposed dividing ratio $< 2^n$), set P_{n-2} or S_{n-1} to logic '1', Eq. (3) can be used to represent the dividing ratio of 'Div_n_vaucher'. If 'S_0' is 0, the binary combination of the adder outputs will be equal to 'm'. The ratio of 'f_{in} / f_{out_origin}' will also be equal to 'm'. After 'Div2', the ratio of 'f_{in} / f_{out}' will be equal to:

$$2 \times m = 0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (4)$$

If 'S_0' is '1', the signal at the input 'C_{in}' of the adder will oscillate between '0' and '1'. The binary outputs of the adder (or the dividing ratio of 'Div_n_vaucher') will have an average value of $0.5 + m$. Thus the average ratio of 'f_{in} / f_{out}' will be equal to:

$$2 \times (0.5 + m) = 1 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (5)$$

Combining Eq. (4) and (5), the dividing ratio can be written as the following:

$$\textit{proposed dividing ratio} = S_0 + S_1 \cdot 2^1 + S_2 \cdot 2^2 + S_3 \cdot 2^3 + \cdots + S_{n-1} \cdot 2^{n-1} + S_n \cdot 2^n \quad (6)$$

The proposed dividing ratio expressed in Eq. (6) is the same as the original one in Eq. (3). So the circuit in Fig. 3 not only generates an output signal with close to 50% duty-cycle, but also keeps the step size of the dividing ratio to be 1 (by changing the control bit "S_0"). The proposed divider could not operate correctly for the isolated division ratios of $2^r - 1$, where "r" is a natural number.

The output duty-cycle of the proposed design can be expressed as:

$$\text{Duty cycle} = \begin{cases} 50\% & \text{when divided by an even number,} \\ \dfrac{k}{2k+1}, & \text{when divided by an odd number } 2k+1 \end{cases} \quad (7)$$

The duty-cycle error = |duty cycle −50%|, which goes down with larger dividing ratios. For example, the duty-cycle error = 5.6% if the divide ratio = 9, and the duty-cycle error = 1% if the divide ratio = 51.

In Fig. 3, the 'Div2', the 'AND' and the 'n bit half adder' circuits are operating at much lower frequencies than the input signal. Thus the duty-cycle correction circuit induces little power penalty, only about 10%. Test results corroborate the effectiveness of the proposed 50% duty-cycle design.

3 Conclusions

A programmable frequency divider with high operating frequency, small layout area, and a wide dividing ratio range has been presented in this paper.

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The divider circuit has been fabricated using 0.18-μm standard CMOS process. Test results show that the programmable frequency divider can operate at 4.5 GHz, which is certainly higher than that of most of the previously published similar works. To improve the driving capability of other circuits, a novel design with 50% output duty-cycle is presented. The new design can still keep the wide dividing ratio range and the dividing-ratio step-size, without increasing the power consumption by much.

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