ELectronics EXpress

IEICE Electronics Express, Vol.4, No.3, 88–93

Synthesis of current mirrors based on evolutionary graph generation with transmigration capability

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Abstract: This paper presents a novel graph-based evolutionary optimization technique called Evolutionary Graph Generation (EGG), and its application to the transistor-level design of analog circuits. The evolution process of EGG can be accelerated by a simple operation, called "transmigration", which is to import previously generated solutions for creating advanced solutions. In this paper, we demonstrate the potential of EGG with transmigration capability through an experimental synthesis of current mirror circuits.

Keywords: evolutionary computation, circuit synthesis, analog circuits, genetic algorithms

Classification: Science and engineering for electronics

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DOI: 10.1587/elex.4.88
Received December 20, 2006
Accepted January 04, 2007
Published February 10, 2007

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1 Introduction

Analog circuits inherently involve trade-offs among a large number of performance metrics, and each performance is determined by the complex and nonlinear nature of relations between the topology and parameter values (e.g., device sizes). It follows that analog circuit design has to be accomplished by the iterative process of three steps: (i) selection of an appropriate circuit topology out of various possible topologies, (ii) minor modification of the circuit topology, and (iii) parameter optimization according to the circuit specification. It requires the knowledge and experience of experts who had trained in a particular way to understand circuit/device technologies.

Addressing this problem, we have proposed a new approach to designing circuit structures using an evolutionary optimization technique called Evolutionary Graph Generation (EGG) [1, 2, 3], and its application to the design of analog circuits. EGG can be regarded as a unique variation of evolutionary computation techniques. Key features of EGG are to employ a graph-based representation of individuals and to manipulate the graph structures directly by evolutionary operations shown in Figs. 1 (a) and (b).

In this paper, we present that analog circuit evolution based on EGG can be accelerated by a simple operation called *transmigration*, which is to import previously obtained good topologies as raw materials in different evolution processes [2]. For analog circuit design, we newly introduce a specific transmigration operation to import both topology and parameter values. Through the design of current mirror circuits, we demonstrate that the transmigration capability can improve the efficiency of EGG-based analog circuit synthesis.

2 EGG with transmigration capability

The circuit structures considered in the conventional EGG consist of only limited kinds of functional nodes. However, there are many important design problems in which a variety of building blocks (i.e., circuit components) with parameter values are to be used to synthesize the target function. Typical examples of such problems include synthesis of analog circuits.

To solve such design problems, we consider a unique possibility of increasing the search efficiency of EGG. The basic idea is to reflect the result of earlier designs into the current evolution process, instead of treating each design task independently. For this purpose, we introduce a new evolution-

DOI: 10.1587/elex.4.88
Received December 20, 2006
Accepted January 04, 2007
Published February 10, 2007

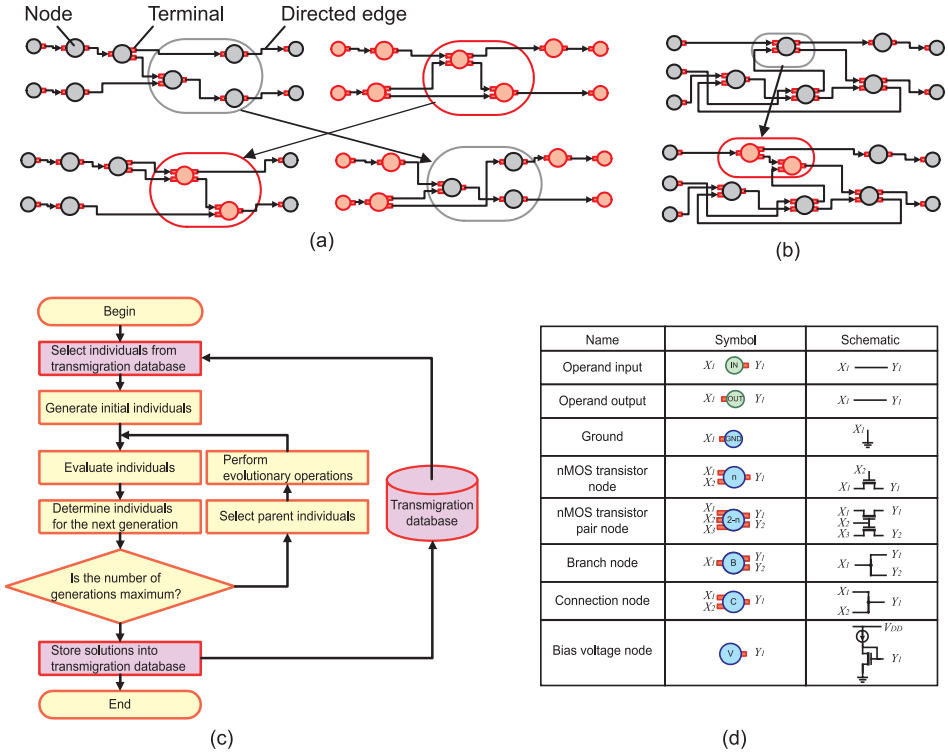

Fig. 1. EGG-based current mirror synthesis: (a) crossover, (b) mutation, (c) EGG system flow with transmigration capability, and (d) functional nodes.

ary operation called transmigration, which is to import previously generated solutions (i.e., circuit topologies associated with parameter values) as raw materials for creating more sophisticated circuits.

Figure 1 (c) shows the EGG system flow with transmigration capability. At the beginning of a new evolutionary run, the system retrieves a set of individuals, which corresponds to previous solutions, from a transmigration database, and merges them with a set of randomly generated individuals to form the initial population. Then, the system performs the evolution process consisting of evaluation, selection, crossover and mutation repeatedly for a specified number of generations. After every successful run, the EGG system stores the solutions in the transmigration database. These structures are accumulated as the knowledge of the system, and be reused on the next evolution process.

3 Synthesis of current mirror circuits using EGG

The design specification considered here is an nMOS current mirror, which is widely used in analog integrated circuits both as a biasing element and as a load device for amplifier stage [7]. The basic function of current mirrors is to produce an output current i_O equal to the input current i_I multiplied by a desired current gain B, that is, $i_O = -B \times i_I$. Ideally the gain B is independent of input frequency, the output current i_O is independent of the output voltage v_O, the input voltage drop v_I equals zero, and the circuit area

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Received December 20, 2006
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is as small as possible.

In practice, the characteristics of real current mirrors deviate from those of ideal ones. There are various possible choices for a current mirror structure due to the trade-offs among the characteristics. We assume here that many advanced current mirrors are composed of a fundamental current mirror, such as cascode and Wilson current mirrors, and its compensation circuit depending on the target specification. The above assumption leads to the idea of transmigration to reuse good subcircuits in the previous solutions.

We have used a set of functional nodes shown in Fig. 1 (d) for synthesizing various current mirrors. Note that each transistor in the node set has the aspect ratio (W/L) as a design parameter, where W and L are the width and length of MOS transistor channel area, respectively. We set $W \in \{0.6\,\mu m, 1.2\,\mu m, \cdots, 3.0\,\mu m\}$ and $L = 0.6\,\mu m$ in this experiment. Thus $(W/L) \in \{1, 2, \cdots, 5\}$.

The generated circuit graph is translated into the corresponding netlist, which is simulated to analyze its electrical behavior and characteristics with SPICE simulations. We define the synthetic evaluation function F as follows:

$$F = \sum_{i=1}^{4} w_i F_i \quad (0 \le F_i \le 1, \quad \sum_{i=1}^{4} w_i = 1),$$

where F_1 evaluates the accuracy in i_I-i_O characteristic, F_2 evaluates the output saturation voltage investigated through DC transfer analysis, F_3 evaluates the settling time obtained from transient response to a step input, and F_4 evaluates the area efficiency. Each F_i takes a value between 0 and 1. $F_i = 1$ shows that the evolved circuit has an acceptable performance for ith characteristic. w_i is a weight coefficient for the ith fitness function, and we set $w_i = 0.25$ for all i in the following experiment.

In order to demonstrate the specific advantage of transmigration, we carry out experiments on generating a variety of current mirrors while tightening the target value of output saturation voltage $\tilde{v}$ gradually in the following order: (i) $\tilde{v} \le 1.5\,[\mathrm{V}]$, (ii) $\tilde{v} \le 1.0\,[\mathrm{V}]$, (iii) $\tilde{v} \le 0.75\,[\mathrm{V}]$ and (iv) $\tilde{v} \le 0.5\,[\mathrm{V}]$. Note that the other target values are set as follows: the error of i_I-i_O characteristic $\tilde{\epsilon} \le 1 \times 10^{-6}\,[\mathrm{A}]$, the settling time for a step input $\tilde{t} \le 1 \times 10^{-9}\,[\mathrm{s}]$ and the circuit area A is as small as possible. We performed 16 distinct evolutionary runs for each condition. Under the first condition ($\tilde{v} \le 1.5\,[\mathrm{V}]$), the proposed EGG system with transmigration capability employs the initial population consisting of circuit graphs which represent simple MOS current mirrors [7] with $(W/L) = 1$ for all transistors. Under the following conditions, the system imports all the solutions generated by previous runs as initial individuals.

The evolutionary run is performed on a 25-node Linux PC cluster, where each node has Intel Xeon 2.8 GHz dual CPUs and 2 GB memory. We employ NGSPICE simulator (a free circuit simulator based on Berkeley's SPICE) for circuit evaluation. Note that we simplify the output format of NGSPICE by program modification, in order to eliminate redundant computational effort. The experimental condition is that the population size is 500, the number

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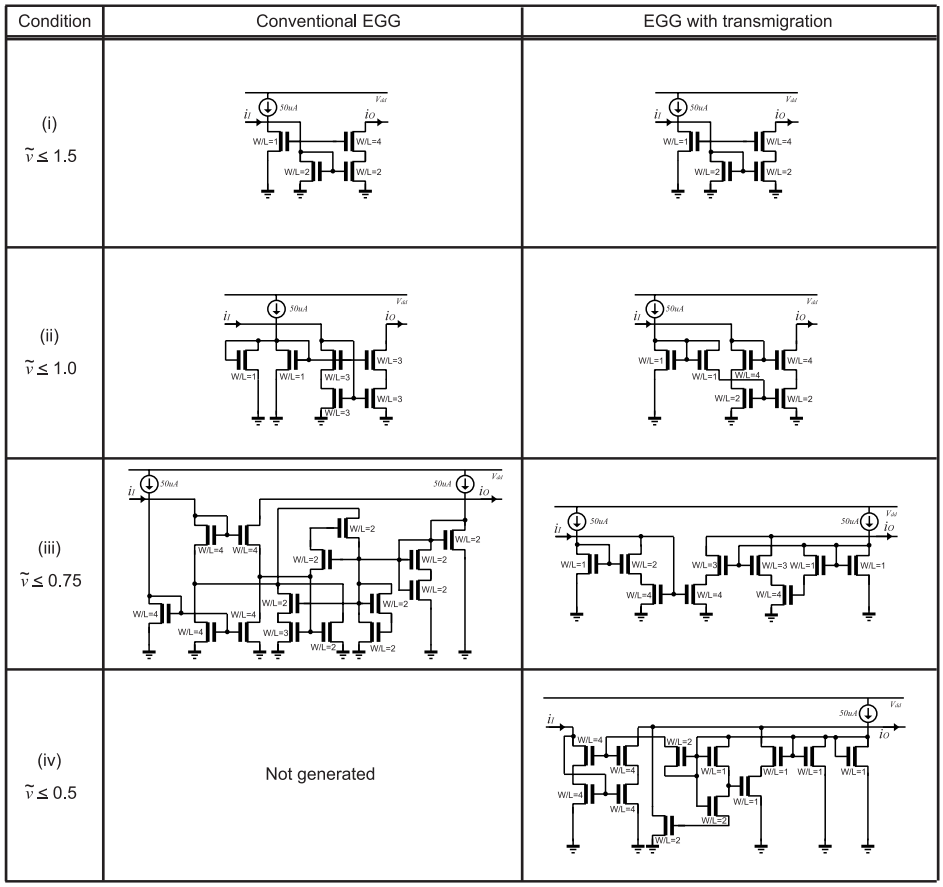
Condition		Conventional EGG					EGG with transmigration				
		$\tilde{\epsilon}$	$\tilde{v}$	t	A	SR	$\tilde{\epsilon}$	$\tilde{v}$	t	A	SR
(i) $\tilde{v} \leq 1.5$	Best	7.8E-07	1.15	4.3E-10	10.2	15/16	7.8E-07	1.15	4.3E-10	10.2	16/16
	Worst	2.0E-06	2.97	5.7E-10	70.1		4.8E-07	1.46	5.9E-10	31.5	
	Ave.	4.1E-07	1.43	7.0E-10	18.1		4.7E-07	1.31	6.4E-10	13.8	
(ii) $\tilde{v} \leq 1.0$	Best	5.8E-08	0.93	7.7E-10	15.4	12/16	4.2E-07	0.96	8.6E-10	15.3	16/16
	Worst	3.3E-06	1.41	9.7E-10	44.8		4.7E-07	0.97	9.7E-10	21.3	
	Ave.	7.6E-07	1.00	7.5E-10	28.7		5.9E-07	0.96	8.2E-10	17.9	
(iii) $\tilde{v} \leq 0.75$	Best	5.3E-07	0.68	8.8E-10	50.2	5/16	6.9E-07	0.70	6.5E-10	25.6	16/16
	Worst	7.9E-07	3.00	7.4E-10	43.5		5.6E-08	0.74	7.9E-10	24.3	
	Ave.	9.8E-07	0.88	8.0E-10	40.8		2.6E-07	0.72	8.8E-10	26.8	
(iv) $\tilde{v} \leq 0.5$	Best	2.3E-06	0.60	8.8E-10	40.7	0/16	9.8E-08	0.46	8.3E-10	31.2	16/16
	Worst	2.5E-06	2.70	1.0E-9	38.6		1.3E-07	0.47	8.7E-10	39.7	
	Ave.	9.9E-07	0.99	8.4E-10	35.0		2.2E-07	0.47	8.5E-10	34.5	

(a)



(b)

Fig. 2. (a) Performance of evolved circuits, and (b) best evolved structures.

of generations is 5000, the crossover rate is 0.7 and the mutation rate is 0.1. 400 individuals are newly generated by evolutionary operations on every generation. Thus, we perform at least 2,000,000 times of SPICE simulations on each run. Using the massively parallel computation on the cluster, we can reduce the execution time for a single run to 1.62 hours on average.

Figure 2 (a) shows the performance of evolved current mirrors, where SR indicates the success rate of generating acceptable solutions on each condition. Figure 2 (b) illustrates the best evolved structures for all the target conditions. The result clearly shows that the proposed EGG system successfully generated more compact and highly-qualified current mirror structures constantly even under the fourth (i.e., the most severe) condition while the conventional EGG system generated redundant circuit structures or some-

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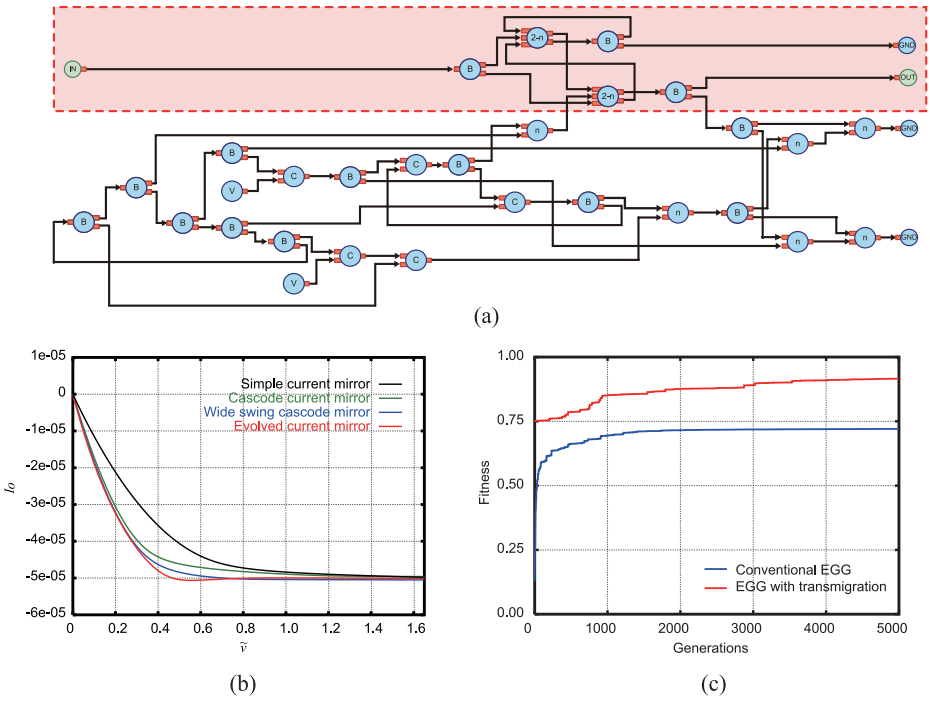

Fig. 3. (a) Evolved circuit graph, (b) v_O-i_O characteristic of evolved current mirror, and (c) average fitness transition.

times failed to generate acceptable solutions. This suggests that the use of the transmigration operation significantly improves the search efficiency of the EGG system.

Figure 3 (a) shows a circuit graph evolved by the proposed EGG system in the fourth condition. We can observe that this circuit graph includes a cascode current mirror, as shown in the hatched portion, and a sophisticated compensation circuit which improves the overall performance. Compared with the conventional current mirrors, this circuit can be driven at lower output saturation voltage (Fig. 3 (b)). Figure 3 (c) compares the average fitness transition of the conventional EGG system and that of the EGG system with transmigration in the fourth condition. We can confirm here that the initial population of the EGG system with transmigration indicates higher fitness value, and the evolutionary search finds the optimal solution more rapidly than the conventional EGG system.

4 Conclusion

In this paper, we demonstrated the potential of EGG with transmigration capability, which successfully generated higher-performance current mirrors. The experimental result suggests a possibility of constructing intelligent circuit synthesis systems, which may evolve its ability by accumulating design experience. By introducing the guidelines for transmigrating suitable individuals, the transmigration operation could achieve more significant results.

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