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A pre-emphasis output buffer control scheme for a GDDR3 SDRAM interface

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Abstract: The keys to good signal integrity in a Graphic DDR3 (GDDR3) SDRAM interface for a bandwidth up to 1.4 Gbps/pin are the minimization of input/output pin capacitance and the accurate control of the output data skew. The proposed pre-emphasis output buffer control scheme provides output data skew minimization without an increase of input/output pin capacitance. Compared to the conventional scheme, the output data aperture window of proposed scheme has increased by 18% and the data output skew has decreased by 48%.

Keywords: GDDR3 SDRAM, termination, signal integrity
Classification: Integrated circuits

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1 Introduction

As operating speeds of computer systems continue to rapidly increase, memory such as DRAM needs to have an increasingly large capacity and operate at increasingly higher rates. Moreover, the required operating frequency of graphic memory, such as Graphic DDR3 (GDDR3) and Graphic DDR4 (GDDR4) is increasing beyond 800 Mhz. In these graphic memory applica-

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tions, the timing margin of the input/output interface is critical to system performance [1]. Most high-speed systems have terminations on board or on the die for the signal integrity of the transmission lines. However, in the graphic memory application, the increase of the data bus width to more than x32 restricts the use of a conventional termination scheme because of power consumption and the power noise problem. To overcome these problems, VDDQ on-die-termination (ODT) has been adopted in GDDR3 SDRAMs. This VDDQ-ODT has an advantage in the reduction of ODT power consumption. VDDQ-ODT, on the other hand, has a serious problem in the symmetric slew rate control of the output data signal. Because the VDDQ-ODT is sensitive to the linearity of the output driver and to the variation of operating voltage, the GDDR3 SDRAM is equipped with programmable impedance output buffers and terminators [2, 3].

The output driver and termination component consist of an active device and passive device to improve linearity of the resistor value. Therefore, the on resistance of the output driver and the termination is the summation of the active device and passive device. To obtain good linearity, the resistance of the passive device is much higher than that of the active device. This configuration leads to an increase of the active device width. In that case, according to the increase of the active device width, the input/output pin capacitance is also increased. To minimize the input/output pin capacitance, the most critical to good signal integrity, an ODT-merged output driver scheme is generally adopted [4].

In this paper, we propose a pre-emphasis output buffer control scheme to improve the signal integrity without an increase of input/output pin capacitance.

2 Pre-emphasis output buffer control scheme

The GDDR3 output driver scheme has a serious problem in the symmetric slew rate control of the output signal. As shown in Fig. 1 (a), when the driver outputs a signal having a logic high state, the DATA signal has a logic high state so that a pull-up transistor is turned on and a pull-down transistor is turned off. Through the pull-up transistor and termination resistor Rtt, the output voltage of the receiver is rapidly increased to a voltage level approximating about VDDQ. When the driver outputs a signal having a logic low state, the DATA signal has a logic low state so that the pull-up transistor is turned off and the pull-down transistor is turned on. Therefore, the output receives a power supply voltage of VSSQ through the pull-down transistor only. The skew may be generated between the rising transition and the falling transition of the output date. Fig. 2 (a) shows the output data transition skew.

To overcome the above problem, we use a conventional scheme to delay an enable signal applied to the output buffer when the output data is driven low relative to when the output data is driven high so that a rising transition and a falling transition of the output data may intersect at the reference voltage

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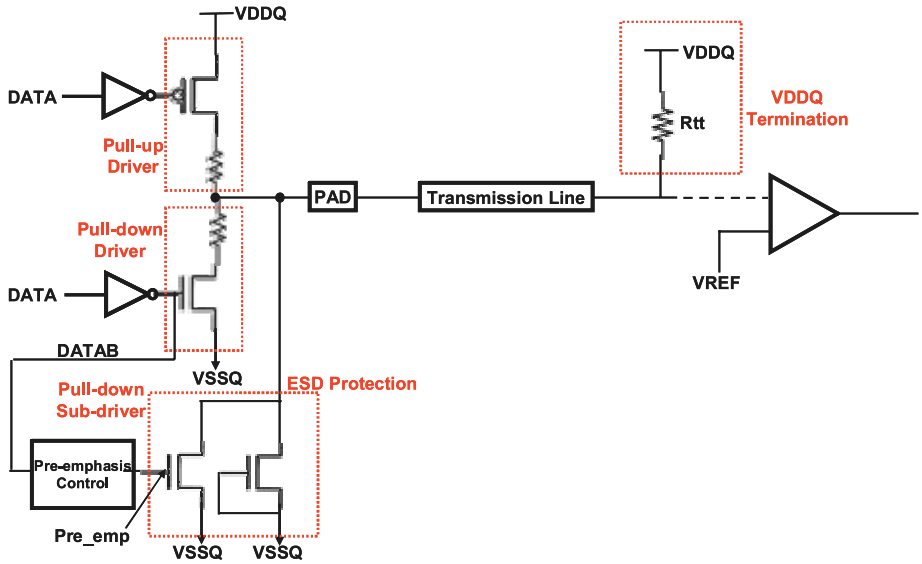
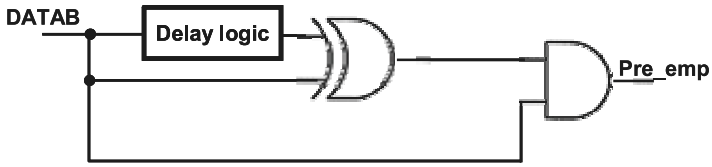
level, VREF. However, the conventional scheme is based on controlled timing so that a predefined amount of delay may vary depending on variances in process, power supply voltage, temperature, etc.

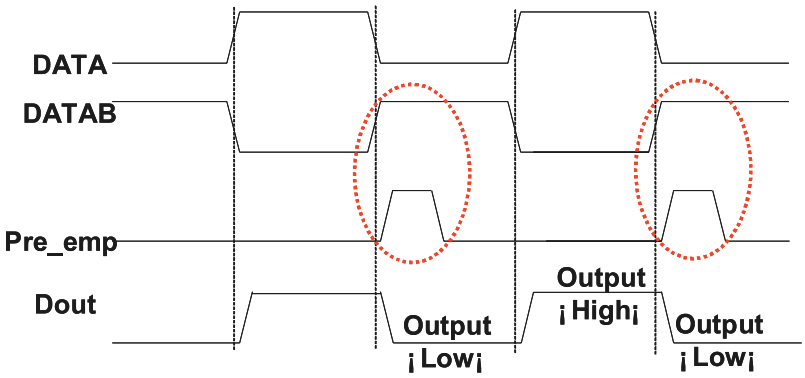
In this paper, we focus on the interface system of a GDDR3 SDRAM. Fig. 1 (a) shows the output driver and receiver termination of the GDDR3 SDRAM. The configuration is comprised of a push-pull driver with a trans-



(a)



(b)



(c)

Fig. 1. A circuit diagram and timing diagram of the proposed output buffer control scheme: (a) a circuit diagram, (b) a block diagram of pre-emphasis control scheme, (c) a timing diagram

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mitter termination, a receiver termination connected to VDDQ, and an ESD protection transistor. The VDDQ-ODT has the advantage of low power consumption. While there is DC current flow between the transmitter and receiver termination when data is low, there is no DC current flow when data is high. This configuration is suitable for the graphic memory interface at the point of power consumption. VDDQ-ODT, on the other hand, has a series problem, like a data transition skew described above. This data transition skew, caused by the output driver and receiver VDDQ termination, limits the maximum operating frequency. The output swing level of the receiver is determined by the ratio of the on resistance between the output driver and the receiver termination. For example, the output low level is determined by the resistance ratio between the terminator and the pull-down driver. In the VDDQ-ODT configuration, the low level of output, V_{OL}, is expressed as the following equation (1) and the high level of output, V_{OH}, is VDDQ.

$$V_{OL} = VDDQ \times \frac{R_{on\_dn}}{R_{on\_dn} + R_{tt}} \tag{1}$$

Herein, R_{on_dn} is the on resistance of pull-down driver and R_{tt} is the on resistance of termination. Therefore, to minimize the data transition skew, the on resistance of the output driver and terminator needs to be precisely controlled.

To solve the data transition skew without an increase of the input/output pin capacitance, we propose a pre-emphasis output buffer control scheme. As shown in Fig. 1 (a), we use a ESD protection transistor together with a pull-down transistor. Fig. 2 (b) shows a block diagram of the pre-emphasis control scheme. Using this control scheme, we generate a short pulse signal to drive the ESD protection transistor.

3 Simulation results

Fig. 2 (a) shows simulation results without the pre-emphasis output buffer control scheme. Fig. 2 (b) shows simulation results when adopting the pre-emphasis output control scheme. Using the proposed scheme, the data transition skew decreased by 48%, and the output data aperture window of the proposed scheme increased by 18%, compared to the conventional scheme. This shows that the proposed scheme is a good approach to reduce the data transition skew without an increase in input/output pin capacitance.

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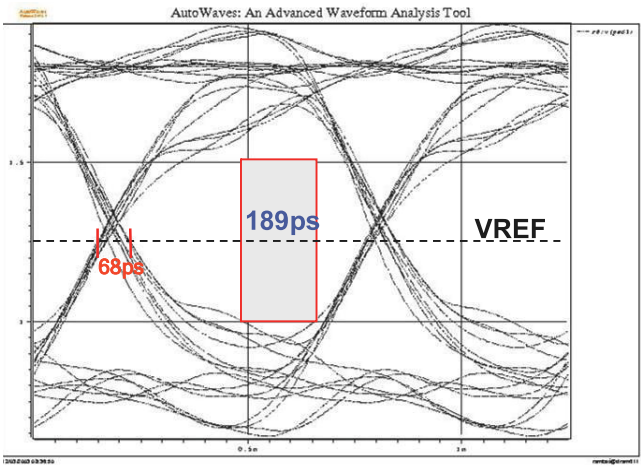
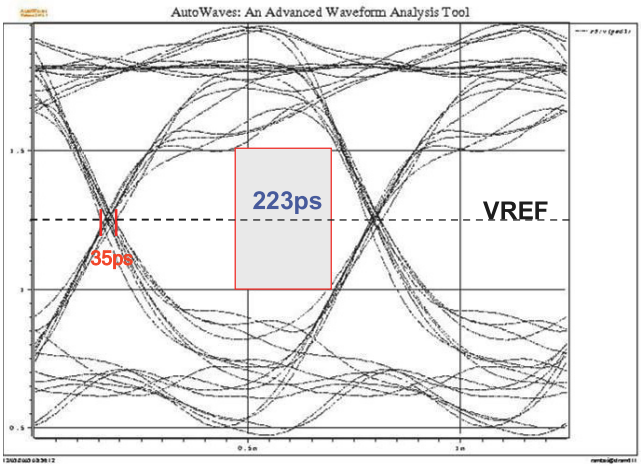


(a)



(b)

Fig. 2. A simulation waveform of the proposed output buffer control scheme: (a) without the pre-emphasis and (b) with the pre-emphasis

4 Conclusion

In the graphic memory application, signal integrity is the most important design consideration. To improve this signal integrity, we need to minimize the input/output pin capacitance and the data transition skew. In this paper, we proposed a pre-emphasis output buffer control scheme and characterized the signal integrity using a computer simulation tool. Through the simulation result, our proposed scheme is a good approach to reduce the data transition skew without an increase of input/output pin capacitance.

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