Standby power reduction using optimal supply voltage and body-bias voltage

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Abstract: This paper proposes a novel design method to minimize the leakage power during standby mode using a novel optimal supply voltage and body-bias voltage generating technique for nanoscale VLSI systems. The minimum level of VDD is generated for different temperature and process conditions adaptively using a look-up-table method. The subthreshold current as well as gate-tunneling and band-to-band-tunneling currents are monitored and minimized adaptively by the optimally generated body-bias voltage. The proposed design method reduces the leakage power by 1000 times on average for IS-CAS85 benchmark circuits designed using 32 nm CMOS technology comparing to the case where the method is not applied.

Keywords: leakage current, standby power, optimal supply voltage and body-bias voltage, nanometer CMOS circuits

Classification: Integrated circuits

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1 Introduction

Due to the continued scaling of the technology and supply/threshold voltage, leakage power has become a dominant portion in the power dissipation of nanoscale VLSI systems [1, 2, 3]. To reduce the leakage power by increasing the threshold voltage of MOSFET transistors during standby mode, adaptive reverse body-biasing (ABB) technique has been proposed [1, 4]. The ABB decreases the subthreshold-leakage current of the scaled MOSFET. However, it increases the depletion width of the MOSFET parasitic junction diode and rapidly increases the band-to-band tunneling current between the substrate and source/drain, especially in halo implants. In addition, the previous techniques require significant circuit modification and performance overhead for leakage reduction, and they have not been complete or robust enough to apply to VLSI systems since all the leakage-current components and minimum supply voltage are not considered for leakage power reduction. This paper proposes a novel circuit technique to achieve low power in standby mode by exploiting the supply-voltage scaling and body-bias-voltage scaling.

2 Optimal body-bias voltage and supply voltage

The main components of leakage power in standby mode are gate tunneling leakage power, sub-threshold leakage power, and reverse biased junction band-to-band-tunneling (BTBT) leakage power [5]. Therefore, the total leakage power in standby mode is given by:

$$P_{leakage} \approx I_{gate}V_{gate} + I_{sub}V_{sub} + I_{BTBT}V_{BTBT} \tag{1}$$

where V_{gate}, V_{sub}, and V_{BTBT} are the voltage sources of each of these leakage current components.

Figure 1 shows the effect of body-bias voltage and supply voltage on the leakage current for a 32 nm NMOS BPTM (Berkeley Predictive Technology Model) with W/L = 128 nm/32 nm and tox = 0.9 nm. In Fig. 1 (a), as the supply voltage decreases from 0.9 V to 0.5 V, and the body-bias voltage (V_{Body}) decreases from 0 V to −2.5 V, the sub-threshold leakage current decreases and the BTBT leakage current increases. The gate leakage current is not significantly affected by V_{Body} as shown in Fig. 1 (b) [5]; however, it is significantly affected by the supply voltage. Therefore, the optimal V_{Body} that reduces the total leakage current, is determined by the relationship between I_{sub} and I_{BTBT}. In [6], I_{sub} and I_{BTBT} are given in simplified form as follows:

$$I_{sub} \approx A_S e^{B_S V_{Body}} \tag{2}$$

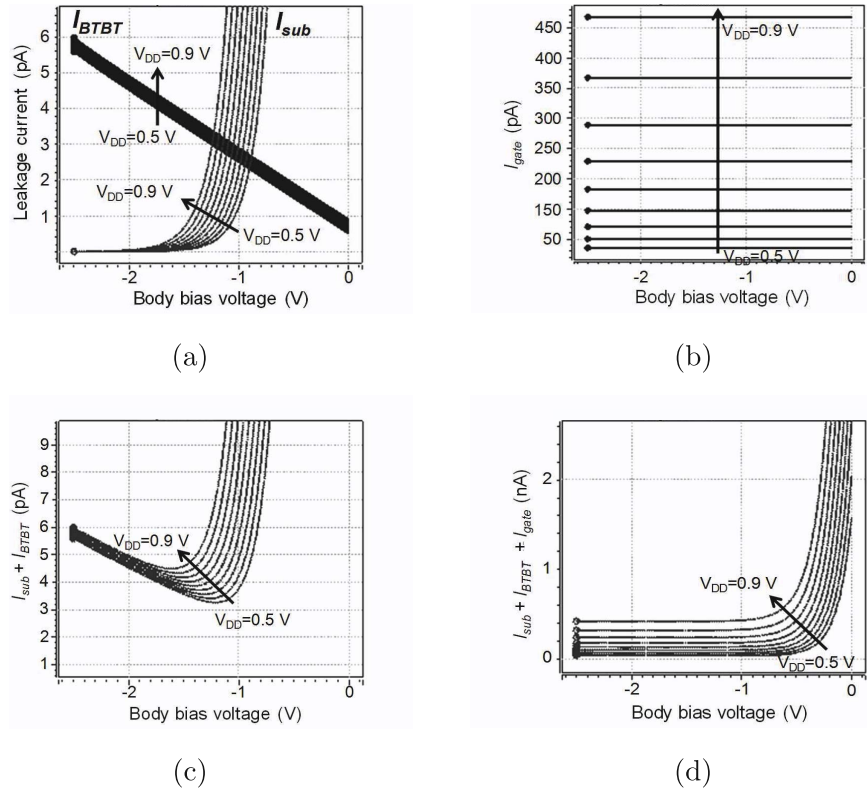$$I_{BTBT} \approx A_b e^{-B_b V_{Body}} \tag{3}$$

Fig. 1. Leakage currents of a 32 nm NMOSFET transistor when $V_{GS} = 0V$ as function of body-bias voltage and supply voltage: (a) I_{BTBT} and I_{sub}, (b) I_{gate}, (c) $I_{BTBT} + I_{sub}$, (d) $I_{BTBT} + I_{sub} + I_{gate}$

where A_b, B_b, A_s, and B_s are the technology dependent constants, and V_{Body} is the body-bias voltage.

The minimal leakage power due to an optimal V_{Body} is calculated by differentiation as in the following equation:

$$\frac{\partial P_{leakage}}{\partial V_{Body}} = 0 \qquad (4)$$

Note that I_{gate} is ignored because the gate tunneling leakage is not sensitive to V_{Body} as shown in Fig. 1 (b). From Eqn. 1, 2, and 4, the condition for minimal leakage power is obtained as follows:

$$B_s I_{sub} = B_b I_{BTBT} \qquad (5)$$

The ratio of B_b and Bs for the minimal leakage current determines the ratio of I_{sub} and I_{BTBT} as given in Eqn. 5. On the assumption that $Bb/Bs = 1$, then I_{sub} must be equal to I_{BTBT} to reduce leakage power. The optimal V_{Body} to reduce the sum of I_{sub} and I_{BTBT} is found from Fig. 1 (c), and it is smaller than V_{Body} to make I_{sub} equal to I_{BTBT}. However, near the value of $-1\,V$ as V_{Body}, the total leakage current $(I_{sub} + I_{BTBT} + I_{gate})$ is almost equal to I_{gate} as shown in Fig. 1 (d), i.e. V_{Body} that makes I_{sub} equal to I_{BTBT}, can be selected as a near-optimal value. The significant leakage component when the body-bias voltage is at the optimal value of V_{Body}, is the gate leakage

I_{gate}, while the supply voltage must be decreased as much as possible to reduce I_{gate}. The reduction of supply voltage decreases the optimal reverse V_{Body} as shown in Fig. 1 (c), while the minimal leakage current is maintained.

3   Circuit Implementation

In the previous section, the optimal V_{DD}/V_{Body} points are found theoretically and through simulations and measurements of a MOSFET transistor. In this section, a novel hardware implementation of the proposed scheme is introduced to adaptively adjust the supply voltages and threshold voltages to minimize the overall power dissipation. This hardware allows the independent adjustment and maintenance of the supply and body-bias voltages when the operating conditions change. The proposed scheme in Fig. 2 (a) consists of look-up table with V_{DD} regulator, leakage monitoring circuit, current comparator, and charge pump.

In the proposed scheme, a look-up table is used to characterize the optimal VDD target for various temperature and process conditions detected. The VDD targets for different temperature and process conditions are derived from simulations or direct measurements of the actual die of interest, whereas the body-bias voltages for NMOSFET and PMOSFET are set automatically
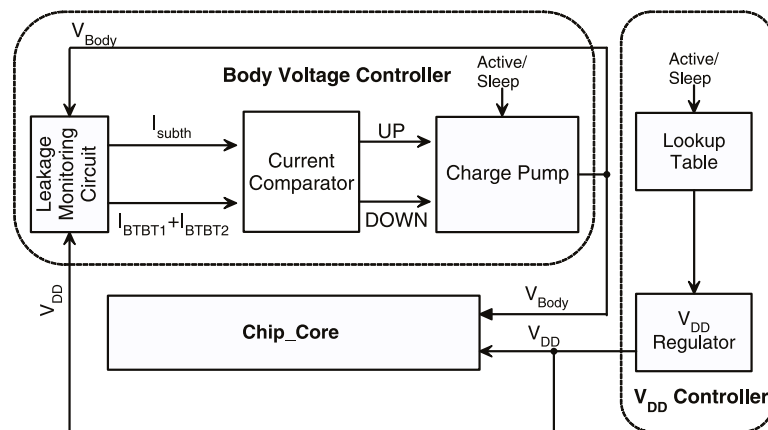
(a)
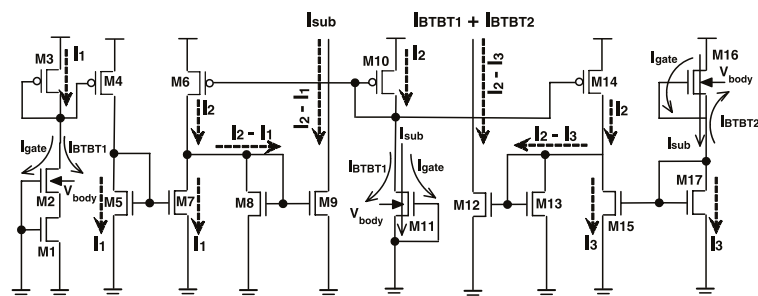
(b)

Fig. 2. Proposed V_{DD} and V_{Body} control system: (a) Block diagram of the total system, (b) Leakage monitoring circuit for the optimal body biasing of NMOSFET transistors

by the control system to ensure that the chip dissipates a minimal power in standby (sleep) mode. The proposed scheme uses current-mode circuit technique to process the active signals in the current domain, and it offers a number of advantages such as better sensitivity, high speed, and low-power dissipation.

A triple-well process is required for the body-biasing technique to control both PMOS and NMOS threshold voltage independently. By applying the reverse bias to the body of the devices, the threshold voltages can be adjusted using the body effect. Therefore, the reverse body biasing (RBB) is often used to reduce the device leakage power. However, if this RBB is too high, the leakage power can be actually increased due to the contribution of the band-to-band tunneling currents. This paper proposes a new optimal body-biasing system to balance the subthreshold leakage with the BTBT leakage. The new system increases V_{th} by adjusting body-bias voltage in the RBB direction so as to reduce the subthreshold-leakage current. When the optimal body-bias point is detected, the body-voltage adjustment is stopped to avoid excessive reverse body bias.

The leakage monitoring circuit separates the subthreshold leakage (I_{sub}) and BTBT leakage current (I_{BTBT}) from total leakage components. Figure 2 (b) shows that the new leakage monitoring circuit extracts exact subthreshold leakage and BTBT leakage components in NMOSFET transistors, where M2, M11, and M17 MOSFET are the replica circuits to generate leakage components, and M3/M4, M6/M10, and M15/M17 form current mirrors. In the drain of M2, I_1 consists of gate-tunneling-leakage current (I_{gate}) and BTBT leakage current (I_{BTBT1}). I_2 in the drain of M11 consists of gate-tunneling-leakage current (I_{gate}), BTBT leakage current (I_{BTBT1}), and subthreshold-leakage current (I_{sub}). In the source of M16, I_3 is generated, and it consists of gate-tunneling-leakage current (I_{gate}), BTBT leakage current (I_{BTBT2}), and subthreshold-leakage current (I_{sub}). The leakage monitoring circuit for PMOS device consists of the same structure as the monitoring circuit for NMOS device.

Based on the generated leakage components, two current differential amplifiers are used to perform subtraction operations. Through M6, M7, and M8, (I_2 - I_1) is obtained, whereas (I_2 - I_3) is obtained through M13, M14, and M15. By these two subtraction operation, ($I_{BTBT1} + I_{BTBT2}$) is obtained in M12, and I_{sub} is obtained in M9. The optimal body-bias point is determined from the two leakage components since the total leakage is minimized when I_{BTBT} equals to I_{sub}. The leakage monitoring circuit of PMOS transistors has almost the same structure as that of NMOS transistors except PMOS replicas to generate leakage currents of PMOS transistors.

The separated leakage components are applied to the current comparator to generate pulse width proportional to the magnitude of each leakage. The current comparator is designed using the current mirrors. The charge-pump discharges or charges its output capacitor depending on two signals from the current comparator and its own bias voltage. The final output stage consists of an opamp and a buffer. The current comparator-based circuit provides

Table I. Experimental results for leakage power

Circuit	# of Gates	With Optimization Typical Corner, T=50°C	Without Optimization VDD=0.9 V, Typical Corner, T=50°C
C432	160	177 nW	11.90 μW
C499	202	230 nW	38.90 μW
C880	383	341 nW	22.00 μW
C1355	546	505 nW	57.20 μW
C1908	880	1436.00 nW	69.86 μW
C2670	1193	3734.00 nW	124.45 μW
C5315	2307	4451.00 nW	180.08 μW
C6288	2388	3900.00 nW	110.64 μW

the optimal body-bias voltage to match the subthreshold leakage with the BTBT leakage currents.

4 Experimental Results

The proposed optimal V_{DD}/V_{Body} control system using 32 nm MOSFET technology (BSIM4 model with 0.9 nm tox) has been implemented and evaluated using ISCAS85 benchmark circuits designed in the same technology. Table I shows the summary of the results for the proposed approach at 50^oC and a typical corner. The average leakage power has been measured using random input test vectors at 0.9 V supply voltage. As shown in Table I, the new technique for the minimal standby power provides average 1000 times reduction in leakage power compared to the simulation results of benchmark circuits without any optimization techniques.

The experimental results demonstrate that the proposed system is very effective and viable in reducing the standby power in the big circuits with the minimal hardware overhead and the minimal power overhead.

5 Conclusion

As technology scales down below 90 nm, the standby power becomes a critical issue. In order to reduce the standby power, this paper presents a novel circuit using the optimal V_{DD}/V_{Body} scaling during standby mode. Based on the predefined lookup table, the optimal supply voltages is generated to reduce the leakage power, and body-bias voltage is automatically adjusted continuously by the control loop. By tuning body-bias voltage using leakage monitoring circuit, circuits can be biased at the optimal point where subthreshold-leakage current and BTBT leakage current are balanced to accomplish the minimum leakage power. The results show that the proposed control system is a viable solution for high energy reduction in nanoscale CMOS circuits.