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A 4-bit 2GSamples/s parallel Flash ADC using comb-type reference ladder

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Abstract: This paper describes a 4 bit parallel flash Analog-to-Digital converter (ADC) using two sub Flash ADCs and comb-type reference ladder. High speed full flash ADCs have been suffered from input referred noise which is noise itself of analog input or noise inferred from reference ladder. As power supply voltage goes lower and resolution goes higher, noise inferred from reference ladder becomes more critical to ADC's performance. The proposed ADC consists of two parallel sub-ADCs with divided reference ladder to overcome degradation due to small reference voltage step. Simulation results show that the proposed ADC achieves 3.96 effective number of bit (ENOB) for 46 MHz input signal and 3.94 ENOB for 1046 MHz input signal at 2 GHz sampling rate. At 2GSample/s, the current consumption is 45 mA including digital logic with 1.8v power supply voltage. The proposed 4 bit ADC is designed with 0.18 um CMOS technology.

Keywords: flash ADC, 4-bit, parallel, comb-type reference

Classification: Integrated circuits

References

[1] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*, John Wiley & Sons, Inc.

[2] Rudy van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, 2nd ed., Kluwer Academic Publishers.

[3] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kutter, "A 6-bit 1.2GS/s low-power flash-ADC in 0.13 um digital CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1499–1505, July 2005.

[4] K. Uyttenhove and M. Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25 um CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1115–1122, July 2003.

[5] P. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s flash ADC in 0.181im CMOS using averaging termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599–1609, Dec. 2002.

[6] Ja-Hyun Koo, Yun-Jeong Kim, Bong-Hyuk Park, Sang-Seong Choi, Shin-Il Lim, and Suki Kim, "A 4 bit 1.356 Gsps ADC for DS-CDMA UWB System," *Solid-State Circuits Conference (ASSCC)*, IEEE Asian, 13–15, Nov. 2006.

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1 Introduction

As the demand of high-speed low power analog-to-digital converter increases, many attempts to achieve high performance with low power consumption [3, 4, 5, 6]. For high speed operation with relatively low resolution ($4 \sim 6$ bit), flash-type ADC seems as a perfect solution. Flash ADCs have suffered from input referred noise and comparator offsets so that averaging techniques have been performed to overcome those problems [5]. And for low power operation, interpolated architecture is used to reduce the number of amplifiers, and also current-mode architecture is used [6]. In this paper, to reduce input referred noise from reference ladder, reference ladder is separated to increase reference voltage step size for better characteristics. With this comb-type reference ladder, two separated flash ADCs operate data conversion respectively and 1/N codes from each ADC are combined to generate full-flash 1/N code in digital logic. From the view of input stage, the proposed ADC seems like two different 3 bit flash ADC, however, after digital operation, the ADC generates 4 bit 1/N code in the end. In this way, with enlarged reference step voltages, the overhead of input stage can be reduced. And with the help of the proposed digital logic, full-flash type ADC is implemented with comb-type reference ladder.

2 Noise Analysis

In parallel type ADC, a number of reference voltages for each comparator level are mostly generated by a resistor network. The input signal is compared with reference voltages to give '1' or '0'. Every comparator generates its own non-correlated thermal noise and these noise sources can result in inaccurate decision, which means wrong decision may occur because of noise [2]. The minimum reference step size in reference ladder can be calculated referred to the noise generated in every comparator. Suppose the noise shows a Gaussian distribution with probability density [1, 2].

$$P(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{\frac{(x-m)^2}{2\sigma^2}} \tag{1}$$

In (1), σ is the standard deviation and can be put equal to the RMS value of the signal (noise). And m is the mean value and is zero in the case of noise [2]. Integration of (1) indicates the probability that the amplitude of a signal is within a pre-determined range. If σ is considered as a large value, an approximation can be used for the integral of the probability density. The one-sided result of this approximation is shown in (2).

$$Q(k) = \frac{1}{\sqrt{2\pi}k} e^{\frac{k^2}{2}} (k \gg 1) \tag{2}$$

Moreover, k gives the number of times a signal is larger than σ. The possibility that the noise amplitude is larger than kσ is determined by 2Q(k). According to [2], the minimum reference voltage step size in a parallel type of converter must be at least between 6 to 7 times of the RMS noise voltage of a comparator. In that case the probability of a decision error due to noise

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tripping of a quantization level is below 10^{-9} with $V_{refstep} = 6\ e_{noise}$. Here e_{noise} is the input referred noise voltage of a comparator plus additional noise of the resistive reference divider.

As mentioned above, for the same reference voltage scale, noise characteristic can be improved when the reference ladder is separated to make reference step size bigger. In other words, for the same reference step size, whole reference voltage scale can be reduced, which is helpful for low voltage operation. Therefore, in this paper, reference ladder is separated that looks like comb to make reference step size twice for the viewpoint from each SubADC.

3 ADC Architecture

In general, an n-bit full flash ADC needs 2^{n-1} reference levels and comparators. For example of 4 bit, reference levels are 15 between Vtop and Vbot. And analog input signal is compared with each reference level to generate thermometer codes. As mentioned above, higher resolution or lower input signal range, reference level step becomes smaller to make ADC hard to operate at high frequency. Higher resolution with high frequency in flash ADC, the interpolated ADC has been achieved to overcome those kinds of problems. The interpolation ADC has several types such as resistor-interpolation at amp output stage or active interpolation using amp stage at output of first amp stage. For example of active interpolation with 4 bit case, the reference levels are 7 between Vtop and Vbot rather than 15, and amps between 1^{st} amps' output generate crossing points between two amps' output. Even though the interpolation ADC improves the noise characteristic at first stage,

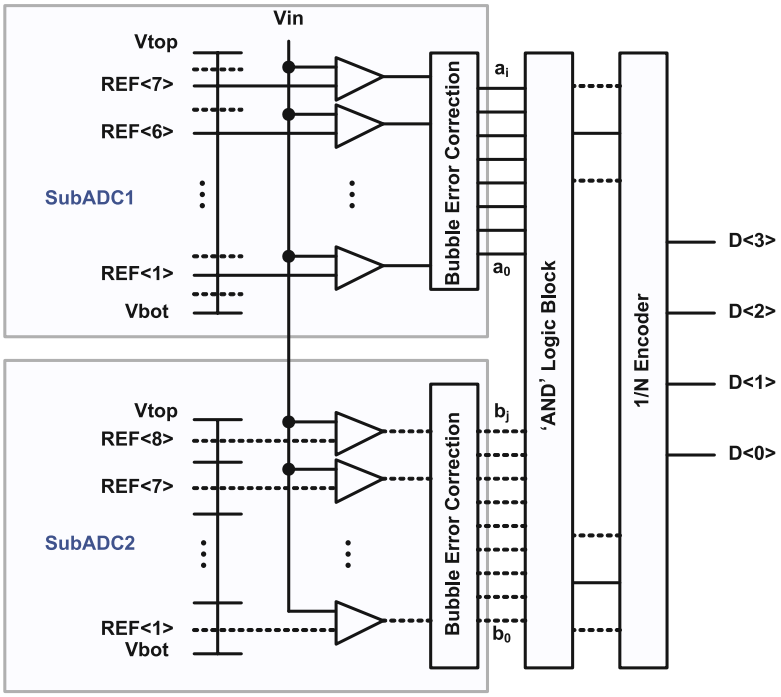

Fig. 1. Block diagram of the proposed Parallel Flash ADC

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it needs lots of interpolation amps after 1st stage so that current consumption increases.

With merits of interpolation ADC at input stage, the parallel flash ADC is proposed in Fig. 1. The proposed ADC consists of two parallel flash-type ADCs. And each ADC has almost half of full reference voltage scale. For example of 4 bit as shown in Fig. 1, among the 2^{4-1} reference levels, even numbers are fed to SubADC1 and odd numbers are fed to SubADC2. For each SubADC, the reference values seemed similar to 3 bit reference signals. With these separated reference values, SubADCs operate data conversion simultaneously and synchronized by main clock signal. After bubble error correction, each thermometer codes are generated from each SubADC. Adjacent codes from each SubADCs are compared by 'AND' logic so that digital logic can generate whole thermometer codes. With newly generated thermometer codes, other digital operations such as encoding and error correction are performed as same as previous architectures. At first amps stage, single input is used rather than fully differential input and reference values are simply divided by 2^n between Vtop and Vbot so that they are not fed to 1st Amps stage differentially. And all digital logics are designed with dynamic logic for high speed operations.

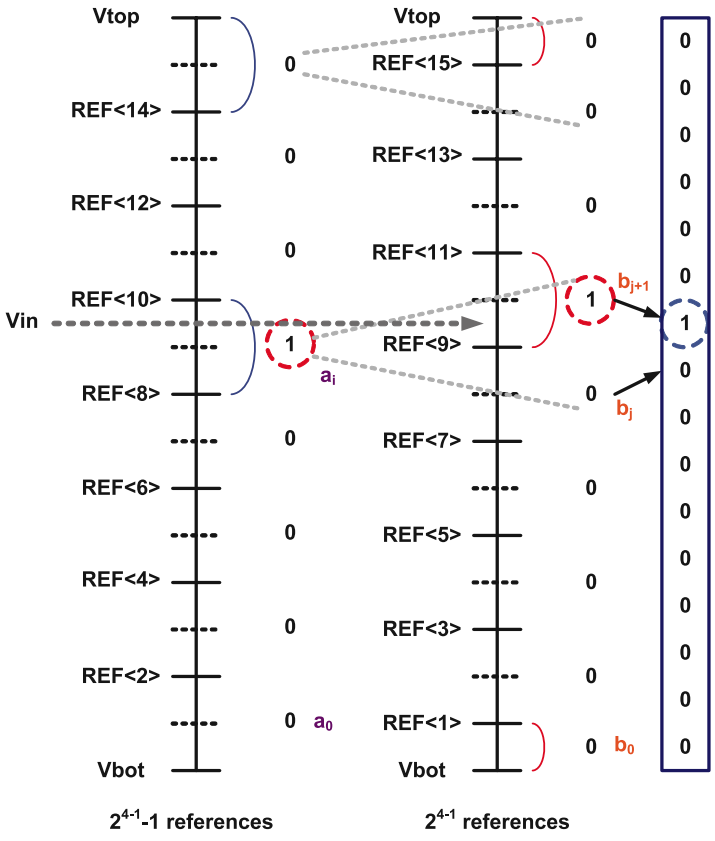

Fig. 2. Concept diagram of the parallel Flash ADC operation

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4 Parallel Flash ADC Conversion

The proposed parallel flash ADC conversion operation is shown in Fig. 2. In Fig. 2, 2^{4-1}-1 reference stage is for SubADC1 in Fig. 1, and 2^{4-1} reference stage is for SubADC2 in Fig. 1. The conversion operation using two reference stages is performed simultaneously in each SubADC. Each SubADC generates thermometer codes to encode 1/N code using bubble error correction digital logic. However, for easy understanding, two reference stages are drawn in series in Fig. 2. For example, input signal is fed between REF<9> and REF<10> as shown in Fig. 2. In SubADC1, one reference step size is the difference between REF<10> and REF<8>, and SubADC1 generates 1/N code at a_i. In SubADC2, same input signal is fed to compare with REF<9> and REF<11>. After 1/N code generation, b_{j+1} code becomes '1'. With these two output codes from each SubADC, 'AND' digital logic operates 'AND' operation of them. From the bottom of 4 bit codes, a_0 AND b_0 becomes the first code, and a_0 AND b_1 becomes the second one. Therefore, final 1/N code for 4 bit is generated by 'AND' operation of a_i and b_{j+1}. And it is the same code generated from full flash ADC if input signal is compared between REF<9> and REF<10> in full flash ADC.

5 Simulation Results

The proposed ADC is designed with 0.18 um CMOS technology with 1.8v supply voltage. As an input signal, single ended 0.6 V_{p-p} sine wave is used. The FFT simulation results of proposed ADC are shown in Fig. 3 (a). At 2GSample/s, the proposed ADC achieves SNDR of 25.59 dB and 25.56 dB for input signal of 46 MHz and 953 MHz respectively. The simulation results of various input signals at 1 GHz and 2 GHz sampling rates are shown in Fig. 3 (b). The current consumptions of the proposed ADC including digital logic are 27 mA and 45 mA for sampling rate of 1 GHz and 2 GHz respectively with 1.8v supply voltage. If the ADC is designed with fully differential circuits, better results can be expected.

6 Conclusion

In this paper, a 4-bit 2GS/s parallel flash ADC is presented. For low voltage and high resolution at GHz sampling rate, we proposed a separated comb-type reference ladder and digital logic for two SubADCs. The ADC is designed using 0.18 um CMOS technology and achieves 3.94 ENOB at the high input signal frequency of 1064 MHz with the current consumption of 45 mA.

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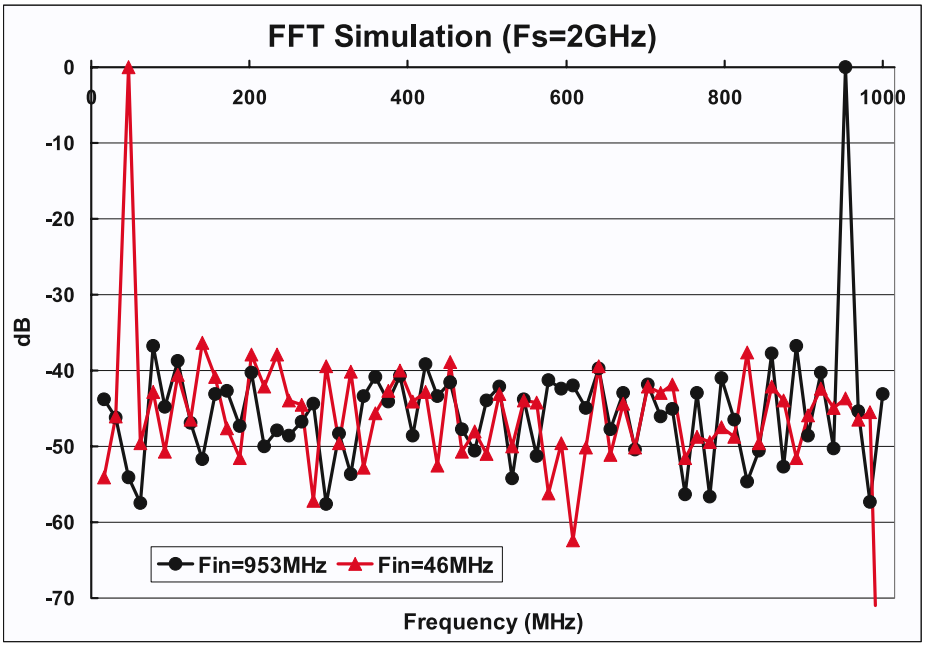
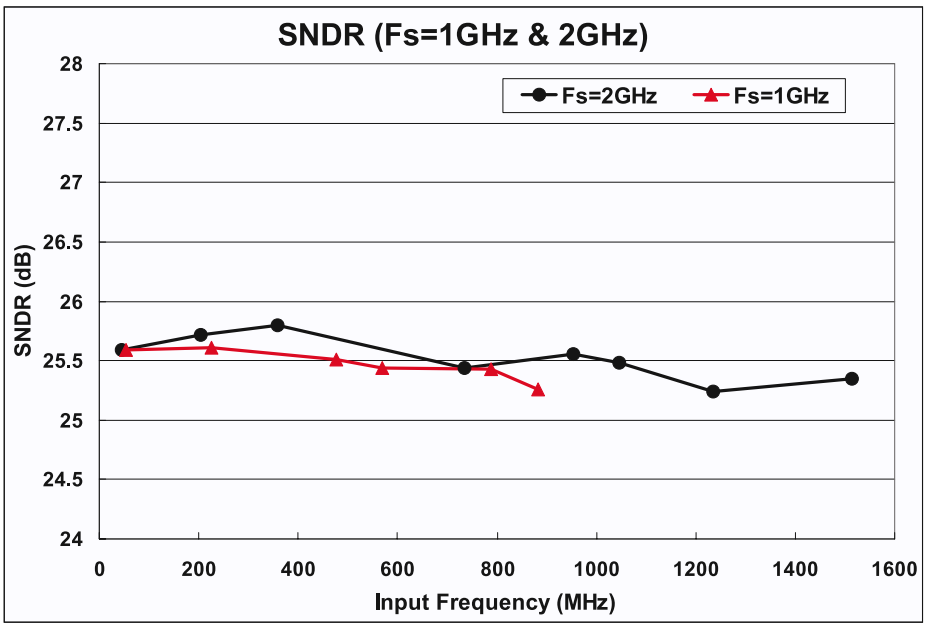


(a)



(b)

Fig. 3. (a) FFT simulation results of the proposed ADC at 2GSamples/s. (b) Simulation results of the proposed ADC

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