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Ultra high speed Full Adders

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Abstract: Two novel 1-bit Full Adder cells based on Majority Function and the similarity between the minterms of the $\overline{\text{Cout}}$ and Sum functions, are proposed. The cells offer higher speed and less Power-Delay Product (PDP) than the conventional and current implementations of the 1-bit Full Adder cells especially in low voltages. All the input patterns are used for simulation to obtain the delay and the power consumption parameters. Simulations demonstrate improvement in terms of PDP and significant improvement in terms of speed.

Keywords: Full Adder cell, high speed, low voltage, Majority function

Classification: Integrated circuits

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1 Introduction

Full Adder is a basic component for all arithmetic operations in the computer structure such as addition, subtraction, multiplication, division, exponentiation and etc. Thus, many designs have been proposed recently to enhance the overall performance of the Full Adder cell [1, 2, 3, 4].

Delay, power consumption and area are the main concerns in designing the Full Adder cells. Propagation of a carry signal to higher bit positions in ripple adders is the most common delay problem. On the other hand, high request of using portable devices strongly demands less area and low power designs. Consequently, the devices will be smaller and the batteries can be used longer. Therefore, enhancing the Full Adder block performance leads to higher system performance [1].

In this paper, we present two novel 1-bit Full Adder cells based on majority function. Carry can be produced by majority structure and the carry itself can produce Sum. Each of these designs is optimized and tested separately in different voltages. Both structures are capable of working perfectly in a vast range of power supply voltages. The delay between the inputs and the outputs of both circuits is considerably short. Results are compared with the following conventional and current Full Adder cells:

1. The conventional CMOS full adder cell [1] which has 28 transistors and is based on the regular CMOS structures (Fig. 1 (a)).

2. The 26T Full Adder cell [2] which has 26 transistors and is based on intermediate XOR/XNOR outputs (Fig. 1 (b)).

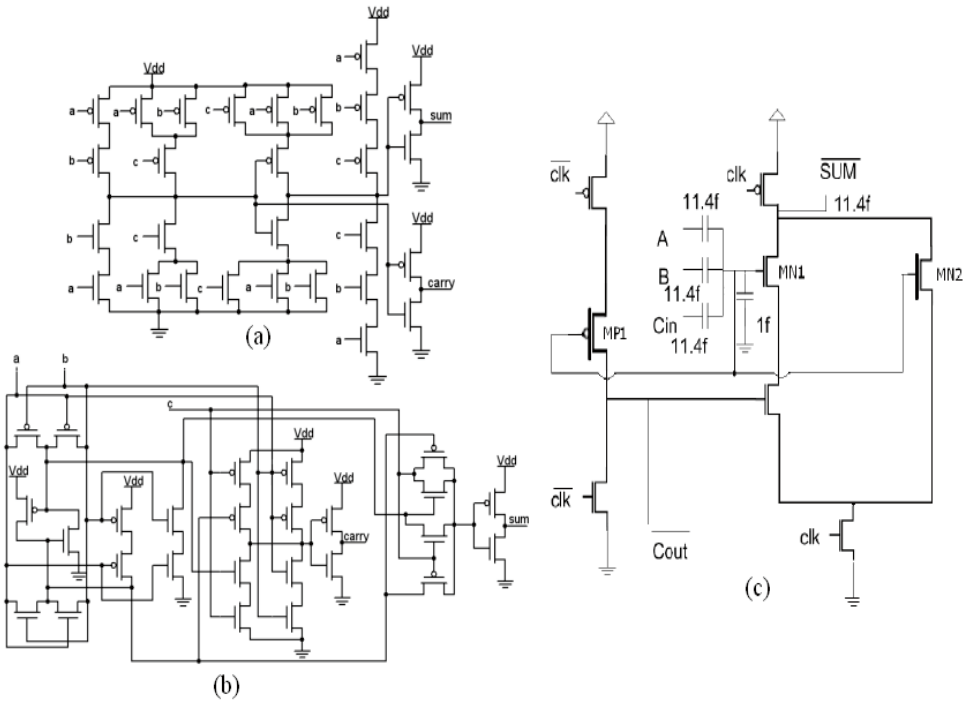

Fig. 1. (a) Conventional CMOS Full Adder cell. (b) 26T Full Adder cell. (c) Dynamic Full Adder cell.

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3. A dynamic Full Adder cell [3] which has 8 transistors and is based on majority function in dynamic logic style (Fig. 1 (c)).

The rest of this paper is organized as follows: In Section 2, we present our two new designs. Then in Section 3, the simulation results are shown. Finally, Section 4 contains conclusion.

2 Proposed Full Adder Cells

The functionality of a Full Adder cell based on Majority Function can be described as follows:

$$\text{Sum} = \text{A} \oplus \text{B} \oplus \text{C}_{\text{in}} = \overline{\text{Maj}(\text{A}, \text{B}, \text{Cin})}.\overline{\text{A}}.\overline{\text{B}}.\overline{\text{Cin}} + \text{A.B.C}_{\text{in}} \quad (1)$$

$$\text{C}_{\text{out}} = \text{Maj}(\text{A}, \text{B}, \text{C}_{\text{in}}) \quad (2)$$

$$\text{Where Maj}(\text{A}, \text{B}, \text{C}_{\text{in}}) = \text{A.B} + \text{A.C}_{\text{in}} + \text{B.C}_{\text{in}} \quad (3)$$

The main idea of both designs is based on the similarity between the minterms of $\overline{\text{Cout}}$ and Sum functions. They only differ in A.B.C_{in} and $\overline{\text{A}}.\overline{\text{B}}.\overline{\text{C}}\text{in}$ minterms. Thus, the Sum function can be created simply by $\overline{\text{Cout}}$ and in the same manner, C_{out} can also produce $\overline{\text{Sum}}$. We have used the second method in the first design while in the second design the Sum function is created by $\overline{\text{Cout}}$. Since majority and C_{out} have same functions, $\overline{\text{Cout}}$ itself can be created by a Majority-Not structure which is easily implemented by only three capacitors and a CMOS inverter gate (Fig. 2 (a) and (b)). The capacitors divide the voltage level of three inputs (A, B and C_{in}) and then the following CMOS inverter will correct the voltage level to V_{dd} if the divided voltage becomes higher than $1/2\text{V}_{\text{dd}}$, and to GND if it becomes lower than $1/2\text{V}_{\text{dd}}$. The two above mentioned minterms are exceptionally produced by using another approach.

2.1 The First Design

The first design (Fig. 2 (a)) has 13 transistors and as a result, it has less area comparing to other designs. Three capacitors, implement the majority structure and the following CMOS inverter enhances the voltage levels and the next node is equal to $\overline{\text{Cout}}$. Since the pull-up and pull-down networks correct the $\overline{\text{Sum}}$ function, the centric CMOS inverter is needed to create C_{out}. The last CMOS inverter enhances the final voltage levels and creates the Sum function.

The switched-on PMOS pass-transistor operates as a resistance. It rectifies the voltage difference in the two exceptional minterms, A.B.Cin and $\overline{\text{A}}.\overline{\text{B}}.\overline{\text{C}}\text{in}$. In these cases, the wrong voltage will be corrected by the pull-up and pull-down networks. In other minterms, both pull-up and pull-down networks are switched off and the majority path creates the Sum output. Since the pull-up passes high voltage and the pull-down passes low voltage, there is no need to change them to transmission-gates.

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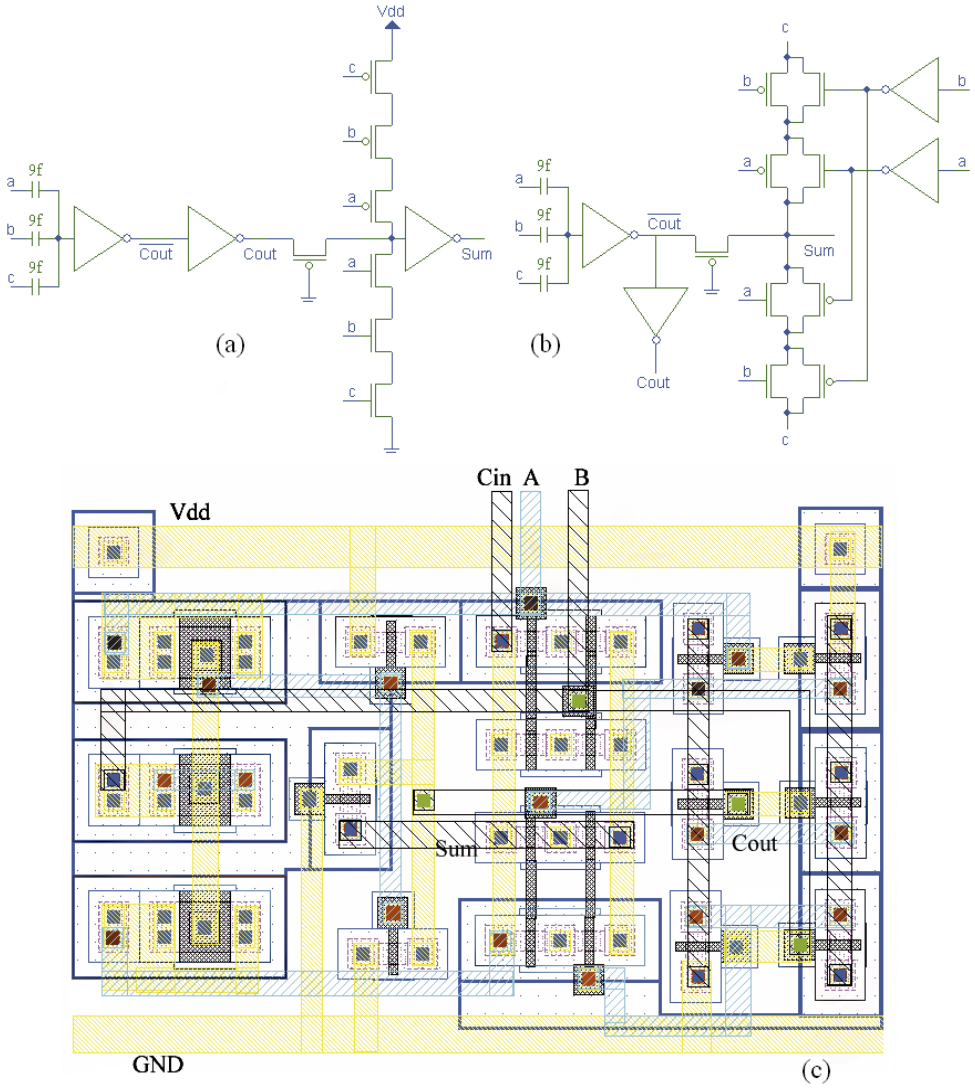

Fig. 2. (a) The first proposed Full Adder cell. (b) The second proposed Full Adder cell. (c) Layout view of the second design.

2.2 The Second Design

The second design (Fig. 2 (b)) is introduced by the aim of enhancing the first design. This design has 15 transistors. This design still has a small area. Delay and power consumption factors have also greatly been enhanced. In this structure $\overline{\text{Cout}}$ creates Sum. New pull-up and pull-down networks are replaced to correct the output in the two exceptional minterms. For better results, we have used transmission-gates which can positively affect the circuit parameters and voltage levels. The usage of the PMOS pass-transistor is the same as in the first design.

Although the second design has 4 more transistors in comparison with the first design, the critical path between inputs and outputs is shorter. In the majority path, the delay of two inverters is eliminated. Also, in the case of switched on pull-up or pull-down networks, the delay of one pass-transistor is removed. Therefore, the second circuit will experience much less delay as

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shown in the simulation section. The layout view of the second proposed Full Adder cell is shown in Fig. 2 (c). As the capacitors are chosen to be 9 fF, the realization is possible with MIMcap and MOScap technologies. MIMcap consumes an enormous chip area while MOScap alternative is not only absolutely realizable but also consumes much less area. The area occupied by a MOScap is nearly as an ordinary transistor, which is very important in reducing the chip area.

3 Simulation Results

Both designs and two other commonly used conventional Full Adder cells (Conventional CMOS and 26T) are all simulated using HSpice with an 0.18 μm CMOS technology at room temperature.

All the possible input transitions are tested to obtain the correct results. The delay parameter is calculated from the time that the input reaches 50% of the power supply level, to the time that the output reaches the same voltage. Rising and falling propagation delays are separately measured for both Sum and C_{out}. Then their maximum is chosen as the delay parameter. The power consumption parameter is the average of power consumption during all the transitions. Finally the power-delay product is the multiplication of the delay of the cell and the average power consumption. Both designs are simulated in a range of power supply from 1.8 v down to 0.8 v. As the dynamic power is proportional to Vdd^2, lowering the supply voltage leads to less power dissipation. Therefore threshold voltage for transistors should be scaled down with the supply voltage [5]. Working with different power supply voltages demonstrates that noise does not affect the functionality of the circuits.

The results for delay, power consumption and PDP are shown in Table I. For instance, by using 0.8 v power supply, the second design is 225% faster than Conventional CMOS and 98% faster than 26T. The PDP of the second design is 1. $1.8442*10^{-16}$ joule which is 128% lower than Conventional CMOS and 65% lower than 26T. The Dynamic Full Adder is the most preferment adder among so many state-of-the-art adder cells [3]. Nevertheless by using 1.8 v power supply, Design2 is 102% faster than Dynamic full adder cell. Dynamic full adder cell is not capable of working properly with power supply voltages below 1.8 v, while the proposed designs can operate properly in

Table I. The results of the proposed designs.

Voltage :	1.8 v			1.2 v			0.8 v		
	Delay * E-12	Power * E-6	PDP * E-16	Delay * E-12	Power * E-6	PDP * E-16	Delay * E-12	Power * E-6	PDP * E-16
Design (2)	82.480	11.595	9.5639	90.905	4.5532	4.1391	98.496	1.8724	1.8442
Design (1)	201.02	9.7732	19.646	230.48	3.9416	9.0846	285.41	1.6236	4.6339
CMOS	225.36	5.9432	13.394	257.61	2.7564	7.1009	320.99	1.3119	4.2111
26T	143.42	7.1063	10.192	161.4	3.2793	5.2929	194.78	1.5579	3.0344
Dynamic	166.3	1.1855	1.971	-	-	-	-	-	-

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lower voltages down to 0.8 v. The best PDP which dynamic full adder cell has ever achieved is with 1.8 v power supply. Comparing the best results of the dynamic and the second proposed cells, the second design is 69% faster and its PDP is 7% lower.

4 Conclusion

Two novel high speed 1-bit Full Adder cells have been presented in this article. HSpice simulations have shown a significant improvement in terms of delay and reasonable improvement in terms of PDP in comparison with other conventional and currently used cells. Both designs were capable of working perfectly in different vast range of voltages. Simulation results have demonstrated that the second design was more efficient than other circuits, considering the parameters of delay and power consumption.

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