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An offset compensated class-AB sample-and-hold amplifier using two sampling capacitors

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Abstract: A new circuit topology of an offset compensated class-AB sample-and-hold (S/H) amplifier using two sampling capacitors is described. Conventional class-AB S/H amplifiers have high power efficiency, but suffer from offset deviations of the internal amplifier. The proposed class-AB S/H amplifier is free from the offset deviation of the internal amplifier, while achieving high power efficiency comparable to conventional class-AB S/H amplifiers. Simulation results show that systematic offset of the proposed S/H amplifier is comparable to that of an offset-compensated class-A S/H amplifier and has faster settling speed than that of the class-A type amplifier.

Keywords: sample-and-hold amplifier, class-AB amplifier, offset compensation

Classification: Integrated circuits

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1 Introduction

Sample-and-hold (S/H) amplifiers are important analog building blocks, especially in data-converter systems, such as pipeline A/D converters and charge scaling D/A converters. Low-power consumption and high-speed sampling are desirable for many applications. Fig. 1 (a) shows a simple S/H amplifier using a single-ended class-A cascode circuit [1, 2]. This circuit is free from the offset of the internal amplifier. The output sink current capability of this circuit is relatively high, but the source current capability is poor, because the pMOS transistor M4 works as a constant current source, while the nMOS transistor M1 works as an active current source. The settling speed is limited by the slewing characteristics of the constant current from M4.

On the other hand, a switched amplifier with capacitive coupling at the input, as shown in Fig. 1 (b), is proposed as a class-AB push-pull operational amplifier [3] that can be used for an S/H amplifier. Similar track-and-hold circuits using floating-gate MOS transistors [4] or floating-gate MOS amplifiers [5] have also been reported. These circuits are expected to have a fast settling time with reduced power dissipation, due to the class-AB push-pull operation. However, these circuits suffer from the offset deviation, due to mismatches between the MOS transistors, e.g., mismatches between the nMOS transistors M1 and M8 or that of the pMOS transistors M4 and M5 shown in Fig. 1 (b). The offset deviation must be minimized if the S/H amplifier is used for array structures.

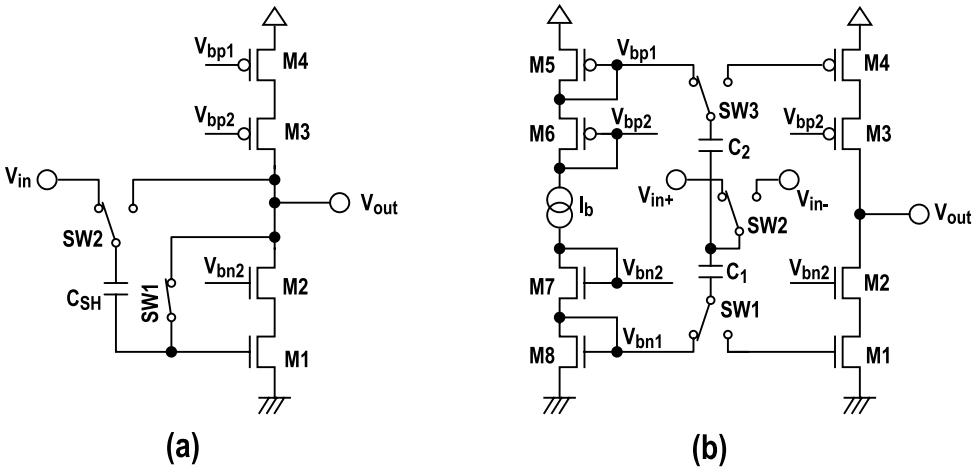

Fig. 1. (a) Conventional class-A S/H amplifier. (b) Class-AB push-pull coscode amplifier from reference [3].

2 Offset compensated class-AB S/H amplifier

Figs. 2 (a) and 2 (b) show the circuits of the proposed class-AB push-pull S/H amplifier in the sampling and holding phases, respectively. At the sampling phase, pMOS transistors M4 and M5 comprise a current mirror and the bias current of the cascode amplifier flowing through M4 is regulated by the

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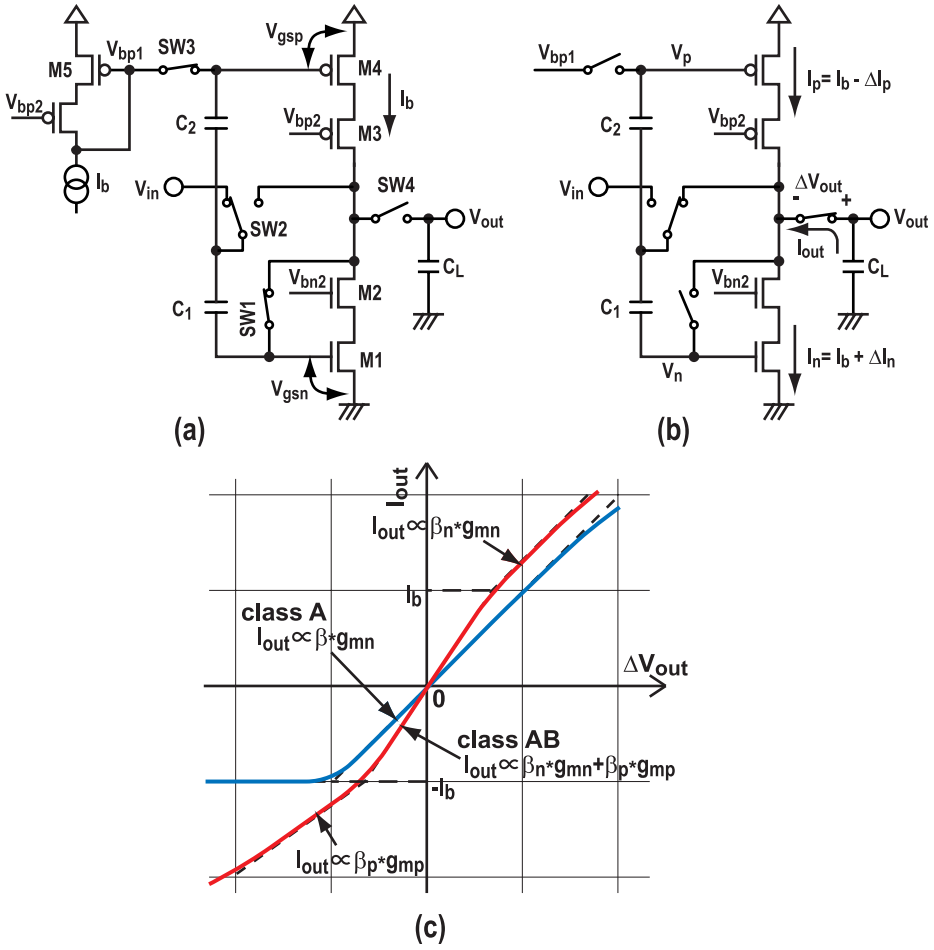

Fig. 2. (a) Sampling phase and (b) holding phase of the proposed class-AB S/H amplifier. (c) Output driving current vs. ΔV_{out}

current mirror. The gate of the transistor M1 is connected to the amplifier output and the input voltage (V_{in}) is given at the mid-point of the series-connected sampling capacitors C_1 and C_2. This operation also memorizes the gate-source voltages of M1 (V_{gsn}) and M4 (V_{gsp}) in C_1 and C_2, respectively. At the holding phase, SW1 and SW3 are turned off and the common terminals of the capacitors are connected to the output by turning SW2 on. The output signal is fed back to both gate terminals of M1, and M4 through feedback factors of $\beta_n = C_1/(C_1 + C_{in})$ and $\beta_p = C_2/(C_2 + C_{ip})$, respectively, where C_{in} and C_{ip} are parasitic capacitances at the gate terminals of M1 and M4, respectively. From the charge conservation law at the gate terminals of M1 and M4,

$$V_{gsn} - V_n = \beta_n(V_{in} - V_{out}) \tag{1}$$

$$V_{bp1} - V_p = \beta_p(V_{in} - V_{out}) \tag{2}$$

are obtained, where V_n and V_p are the gate terminal voltages of M1 and M4 in the holding phase, respectively. The cascode amplifier used in Fig. 2 (b) is driven by both M1 and M4, so that the output V_{out} is given by

$$V_{out} = V_{gsn} + G_n(V_{gsn} - V_n) + G_p(V_{bp1} - V_p) \tag{3}$$

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where G_n and G_p are the open loop gains due to the gate inputs of M1 and M4, respectively. From Eqs. (1), (2) and (3), the output in the holding phase is given by

$$V_{out} = \frac{V_{gsn} + (G_n\beta_n + G_p\beta_p)V_{in}}{1 + G_n\beta_n + G_p\beta_p} \approx V_{in} \tag{4}$$

if $G_n\beta_n + G_p\beta_p \gg 1$. Therefore, if the open loop gain of the cascode amplifier is sufficiently large, then offset-compensated S/H operation is realized.

This circuit has another switch SW4 to avoid returning the output voltage V_{out} to V_{gsn} at every sampling phase. When SW4 is turned on in the holding phase, the deviation of the output from the sampled signal voltage generates the output current I_{out} to drive the load capacitance C_L. Fig. 2 (c) shows the output current characteristics of the class-A S/H amplifier (Fig. 1 (a)) and the class-AB amplifier (Fig. 2 (b)) at the holding phase. If the output voltage deviation from the sampled signal voltage is small, then the output current of the class-AB amplifier is given by

$$I_{out} = (\beta_n g_{mn} + \beta_p g_{mp})\Delta V_{out} \tag{5}$$

where g_{mn} and g_{mp} are the transconductance of M1 and M4, respectively, and ΔV_{out} is the output voltage deviation from the sampled signal voltage. Therefore, the output current is linearly driven by the output voltage for both polarities of ΔV_{out}. However, if ΔV_{out} exceeds either the overdrive voltage of M1 or M4, then M1 (or M4) is cut off and the output current is driven by either M4 (or M1). The resulting characteristic of the class-AB S/H amplifier is shown by the red line in Fig. 2 (c). Faster settling can be realized in the class-AB S/H amplifier, because of this high output current drivability. On the other hand, for the class-A S/H amplifier, the output current is limited by the bias current I_b, for a large negative output voltage deviation, as shown by the blue line in Fig. 2 (c).

3 Simulation results

The DC characteristics and transient behavior of the two circuits shown in Figs. 1 (a) and 2 (b) are designed and simulated using SPICE with 0.25 μm CMOS technology. The same cascode amplifier with a bias current $I_b = 100\,\mu A$ is used for both circuits. The sampling capacitors C_{SH} in Fig. 1 (a) and C_1,C_2 ($C_1 = C_2$) in Fig. 2 (b) are chosen as 1 pF and 0.5 pF, respectively, in order to maintain the same total sampling capacitance. Fig. 3 (a) shows the simulation results for the systematic offset voltage as a function of the input voltage. Both circuits have similar offset voltage that vary from 0.7 to -1.0 mV for the input range of 0.4 to 2.1 V. The offset variation is mainly caused by the finite gain of the cascode amplifier, which is 62 dB in this design. Fig. 3 (b) shows the transient response of both circuits when input voltages of 0.75 V and 1.75 V are alternatively sampled. The rising response of the class-AB S/H amplifier (red line) is much faster than that of the class-A type (blue line). The settling time, to meet the settling error of 1 mV, for inputs of 1.75 V and 0.75 V, is 18.3 ns and 36.3 ns at rise and 12.3 ns and

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15.1 ns at fall, respectively, for the class-AB and class-A S/H amplifiers. This result indicates that the settling response of the class-AB S/H amplifier is improved not only for rise time, but also for fall time.

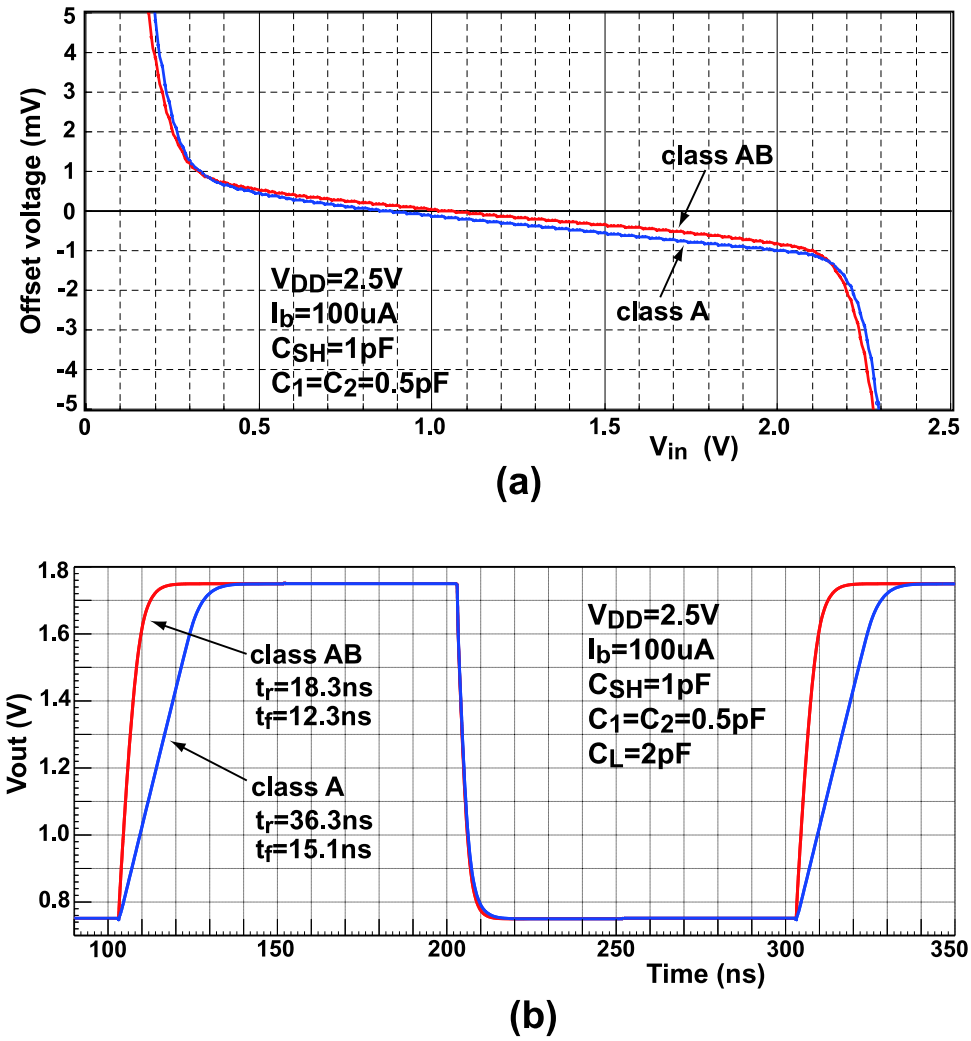

Fig. 3. (a) Offset voltage as a function of input voltage V_{in}. (b) Transient response of the class-A and the class-AB S/H amplifier.

4 Conclusion

An offset-compensated class-AB S/H amplifier was proposed, and the systematic offset characteristics and the settling behavior, were simulated to demonstrate the comparable offset and faster response when compared with a class-A S/H amplifier. The proposed circuit is useful for application to an S/H array that requires low-power dissipation. This circuit topology can also be applied to fully-differential S/H amplifiers.

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