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Selective scan slice repetition for simultaneous reduction of test power consumption and test data volume

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Abstract: In this paper, we present a selective scan slice encoding technique for power-aware test data compression. The proposed scheme dramatically reduces test data volume via scan slice repetition, and generates an adjacent-filled test pattern known as the favorable low-power pattern mapping method. Experiments were performed on the large ITC'99 benchmark circuits, and results show the effectiveness of the proposed method.

Keywords: design-for-testability, low-power testing, scan testing, test data compression

Classification: Science and engineering for electronics

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1 Introduction

Test data compression may give a promising solution for improving test efficiency of scan-based test application. Huge test data can be compressed

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using specific test data encoding techniques, and the original test patterns are decompressed to many scan chains using a few automatic test equipment (ATE) channels. Therefore, both test data volume (TV) and test application time (TAT) can be efficiently reduced by test data compression techniques. However, modern testing environment should consider another important factor; power consumption. During normal mode, functional patterns are highly correlated to generate meaningful output data. However, test patterns generated from automatic test pattern generation (ATPG) process are produced without any correlation of the successive test patterns. Therefore, the uncorrelated test patterns contribute to higher switching activity which may lead to the structural damage due to the higher power consumption than functional patterns [1]. Consequently, future test data compression should minimize TV and TAT while it also minimizes the number of switching activity.

Among test data compression methods, selective scan slice encoding technique [2] presents high TV and TAT reductions. However, [2] does not consider power-aware test data decoding, and [3] is the power-aware version of [2]. In [3], three X-filling heuristics, 0-filling, 1-filling, and adjacent-filling techniques are adopted. With some loss of compression ratio, it generates power-aware test patterns. However, too much loss or no compression effect cannot be obtained when the adjacent-filling heuristic is applied, even though the adjacent-filling technique is known as the favorable power-aware X-mapping heuristic.

The contribution of this paper is the power-aware test pattern generation with low TV and TAT. The proposed method is based on the scan slice repetition technique [4]. After decoding the encoded data, the adjacent-filling test patterns are inserted to the scan chains with high test data compression ratio.

2 Proposed encoding technique

The proposed scan slice repetition technique is based on the selective scan slice technique. In the conventional method, a logic value is broadcasted to scan chains if the scan slice is constant which means that it can be made with a single logic value. Therefore, simple encoding is possible for the constant scan slice. However, complicate encoding and decoding procedures are required, if the scan slice is not constant. In this case, a dominant logic value is encoded, and each conflict bit which is specified as the inverse value of the dominant value should be encoded with separate encoding data. Using this method, high compression ratio can be obtained. However, the conventional method is inadequate to encode adjacent-filling patterns due to the nature of the adjacent-filling heuristics. In the conventional technique, the unspecified bits are filled with logic 0 or 1 based on the number of 0-specified or 1-specified bits of the scan slice to make a constant scan slice and minimize the number of conflict bits. Therefore, they care only about the vertical information of the scan slice, but the logic values should be assigned based on the

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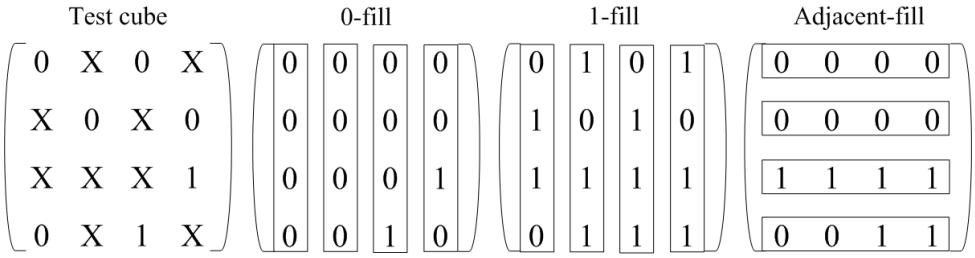
horizontal information to effectively encode the adjacent-filling test pattern. An example of test set and its X-filling results are described in Fig. 1 (a). As shown in Fig. 1 (a), 0-filling and 1-filling techniques can be performed without any information of the successive scan slices, and 2 and 5 conflict bits exist, respectively. However, adjacent-filling technique fills don't-care bits based on the previously specified logic values, so the number of conflict bits increases as 6 by applying the conventional selective scan slice encoding methods. These conflict bits are major contributor of the large test data volume and should be minimized. To minimize the number of the conflict bits, the proposed scan slice repetition technique encode test data based on the previous scan slice. Figure 1 (b) presents the proposed test data encoding method for test cube shown in Fig. 1 (a). The size of encoding data is defined as $\lceil \log_2(N+1) \rceil$, where N is the number of scan chains which is the same with the size of scan slice. Therefore, 4-bit scan slice requires 3-bit encoding data. Encoding data 000 is reserved for repeating present state and 001 to 111 point conflict bit to be reversed. In Fig. 1 (b), 0XX0 should be made as 0010 for applying adjacent-filled test data as shown in Fig. 1 (a). Since the initial scan slice is assumed as 0000, the 3rd bit is encoded as 0010 to reverse third bit and 0010 can be applied by repeating the present state. Next, scan slice X0XX can be simply encoded by repeating the present scan slice, since the present scan slice 0010 is compatible with X0XX. The remaining scan slices can also be encoded with the same encoding criteria, and the number of conflict bit is reduced from 6 to 2 by adopting the proposed test data encoding method.

The detailed encoding algorithm of the proposed scan slice repetition technique is as follows. For the given test patterns which are prepared to apply N scan chains, the size of encoded data is defined as $\lceil \log_2(N+1) \rceil$



(a)

Scan slice	Present	Encoded data	Next	Description
0XX0	0000	011	0010	reverse 3rd bit
	0010	000	0010	repeat present state
X0XX	0010	000	0010	repeat present state
0XX1	0010	100	0011	reverse 4th bit
	0011	000	0011	repeat present state
X01X	0011	000	0011	repeat present state

(b)

Fig. 1. Diverse X-filling heuristics and the proposed encoding technique

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and the present scan slice is initialized as all 0 s. After that, each scan slice is sequentially analyzed, and the position of the conflict bit is encoded if the scan slice is incompatible with the present scan slice. After encoding all the position of each conflict bit, the all logic 0 is additionally encoded for repeating the present scan slice for applying the scan slice to the scan chains. The encoding procedure is completed when every scan slice is encoded under these criteria.

3 Decompression architecture

To decode test data encoded with selective scan slice repetition technique, the overall on-chip decoder is implemented as presented in Fig. 2 (a). When N is the number of scan segments, the first scan cells on each scan segment are implemented as the N-bit scan input repeater cells that hold or reverse the present scan slice. N scan segments are numbered from scan segment 0 to scan segment N-1, and the scan input of i-th scan segment is connected to i-th scan input repeater cell ($0 \leq i \leq N$-1). N-bit repeat signals are utilized as the inputs of the N-bit scan input repeater cells, and generated by the decoding logic. Select signals are required to distinguish $N+1$ states, so the bit width of select is determined as $n = \lceil \log_2(N+1) \rceil$. The N decoding states are for distinguishing each scan input repeater cell, and the additional state is for presenting the repeat state. When implementing the decoding logic, it can be implemented as combinational logic based on the n:(N+1) one-hot decoder. and Fig. 2 (b) shows i-th scan input repeater cell which is attached to i-th scan chain ($0 \leq i \leq N$-1). Therefore, N scan input repeater cells are required for configuring the on-chip decoder. Data-in (DI), Data-out (DO), and Scan enable (SE) are required for the normal scan operation. Repeat (rpt) signal is additionally assigned to apply scan input data using the proposed method. If reset is 0, then D flip-flop is initialized as 0. Additional initialization is not required, since the present value is always known by ATPG. Subsequently, D flip-flop holds or reverses its present value by the repeat signal. If the repeat is logic 0, then the scan input repeater cell holds the present value. And the scan input repeater cell reverses the present value when the repeat is logic

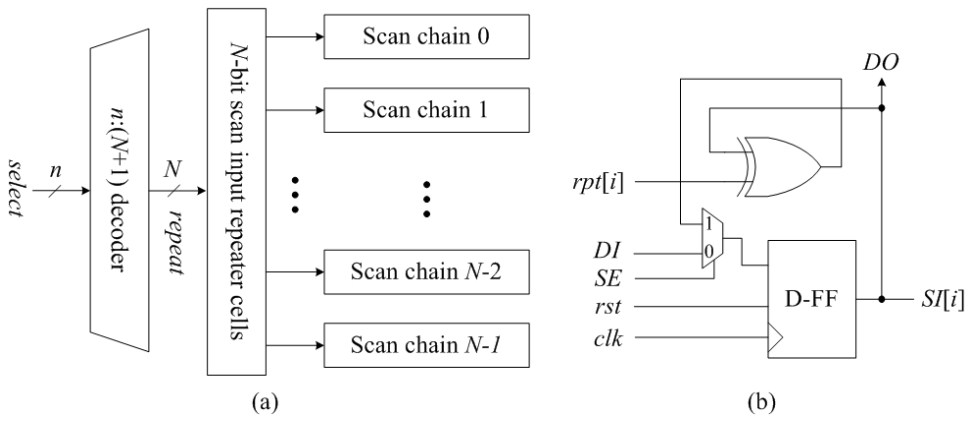

Fig. 2. Selective scan slice repetition architecture

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1. Based on the scan input repetition, test power can be effectively reduced, since the adjacent-filled test vectors are applied to each scan chain.

4 Experimental result

To verify the effectiveness of the scan slice repetition technique, we performed experiments on the large ITC'99 benchmark circuits in terms of the test data volumes and power consumptions. Each circuit was synthesized by Design Compiler of Synopsys and the test patterns were generated byTetraMax of Synopsys. The main features of the three ITC'99 benchmark circuits, b17, b18, and b19 are as follows. The number of scan cells of b17, b18, and b19 is 1,317, 3,064, and 6,130, and the number of scan patterns of them is 678, 4,652, and 11,483, respectively. Table I presents the comparison of test data volume and power consumption. In Table I, SC, CH, T_E, WSA denote the number of scan chains, the number of ATE channels, the encoded test data volume, and the number of WSA, respectively. To enhance test data compression ratio, [3] assumed the ATE pattern-repeat technique. However, it is not applied in our experiments, since it can be applied not only to [3] but also to any test data compression technique. Moreover, it requires the special memory architecture of ATE to enable operations like loop and jump. Therefore, a simple comparison of the compressed test data volume with the ATE pattern-repeat technique is not adequate to estimate the performance of the test data compression technique. At first, the test data volumes of the proposed method are far smaller than those of [3] for any X-filling heuristics as shown in Table I. Since the proposed method encodes test data based on the horizontal information of successive scan slices. Therefore, the number of conflict bits can be minimized using the proposed method. However, [3] cannot effectively reduce the number of conflict bits, since it encodes test

Table I. Comparison of test data volume and power consumption

Circuits	SC	[3]				Prop.	
		CH	T_E(b)			CH	T_E(b)
			0-fill	1-fill	Adj.-fill		
b17	255	10	335,510	345,460	493,040	8	221,024
	511	11	301,378	298,012	360,382	9	236,763
b18	511	11	2,394,513	3,543,101	4,003,791	9	1,498,626
	1023	12	2,136,864	2,258,664	2,787,000	10	1,542,210
b19	1023	12	7,486,728	8,033,676	13,116,672	10	4,574,320
	2047	13	6,856,629	7,266,389	9,188,400	11	4,625,148
Circuits	SC	CH	WSA			CH	WSA
			0-fill	1-fill	Adj.-fill		
b17	255	10	76,942	81,274	55,567	8	55,567
	511	11	30,367	33,094	22,707	9	22,707
b18	511	11	486,427	539,602	340,591	9	340,591
	1023	12	199,792	211,156	132,125	10	132,125
b19	1023	12	1,348,927	1,547,652	960,672	10	960,672
	2047	13	534,598	619,026	373,557	11	373,557

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data based on the vertical information.

Next, Table I also shows the comparison of the total number of switching activities. In [3], 0-filling and 1-filling techniques reduce considerable power consumption, but the proposed method shows the better reduction of the number of switching activity. As presented in Table I, WSA of the proposed method and that of [3] is the same when the adjacent-filling heuristic is applied, however, the test data compression ratio of [3] is very poor when adjacent-filling is applied as shown in Table I. Therefore, the proposed method requires smaller test data volume and power consumption than [3], and these can maximize the test data compression efficiency.

5 Conclusion

In this paper, we presented a power-aware test data compression technique. To reduce test data volume and power consumption, we proposed the test data encoding scheme using scan slice repetition. The adjacent-filled test patterns, which is known as the most favorable low power test pattern, are generated by decoding the encoded data. To obtain adjacent-filled test patterns, the test patterns are compressed based on the information of the successive scan slices. By maximizing the compatible probability based on the scan slice repetition, a high test data compression ratio is obtained. Experimental results show that the proposed technique simultaneously minimizes both test data volume and switching activity. Moreover, the simple on-chip decoder requires a low number of ATE channels. Therefore, efficient low power test data compression can be achieved with a small amount of ATE memory using the proposed technique.

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