

FPGA-based field-oriented control for induction motor speed drive

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Abstract: In this paper, a flexible, high computation speed and cost effective field programmable gate array (FPGA)-based speed controller for an induction motor with field-oriented control, (FOC) is presented. All the control functions including the space vector modulation based PWM waveform generation, field-oriented control algorithm and rotor flux position estimation have been realized using FPGA to reduce the total part count of the hardware prototype and hence provide a low cost solution. The constructed FOC IC consists of 6844 logic elements and is realized using Cyclone, EPIC12q240C8 from Altera Inc. The sampling rate can be programmed up to 100 MHz. Experimental result is included in this paper to illustrate the performance of the designed IC, FOCIC and the feasibility of integrating of SVM and FOC on single chip.

Keywords: FPGA, field oriented control, induction motor drives

Classification: Science and engineering for electronics

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1 Introduction

Most of the ac drives in use today were adopting either fully DSP based digital control strategy or partially FPGA and DSP as reported in [1, 2, 3, 4]. No doubt, this arrangement has the advantages of simpler circuitry, software control and flexibility in adaptation to various applications; it suffers the disadvantages of sluggishness and limited computation resources due to the sequential computation feature, complicated design process and long development time cycle [5]. Of course, multiple DSPs can alleviate this problem at the expense of high cost. On the other hand, the recent advancement of ASIC based devices such as field programmable gate array, FPGA developed by Altera Inc has provided an economic solution and fast circuit response due to its simultaneous instead of sequential execution. Also it is very convenient for laboratory implementation of a project due to its unique hardware reconfigurable feature. Therefore the implementation and circuit realization using FPGA for SVM IC design has been reported in many papers [5, 6, 7, 8, 9]. This paper has focus on the design and development of a flexible and cost effective FPGA based IC for AC motor drives, which incorporate the FOC with SVM algorithm in a single chip, FOCIC. Recently a similar design implemented using dspIC30F6010A from Microchip has been reported in an application notes, AN1078 [13]. Similar to DSPs solution, the execution speed is limited by sequential execution and its maximum external oscillator frequency of 40 MHz [14]. Even with maximum 10 MHz oscillator input with

PLL set to 16x, its instruction cycle is limited to $(10 \text{ MHz} * 16) / 4 = 40 \text{ MHz}$. Whereas the sampling rate of the FOCIC can be programmed up to 100 MHz and its ability of simultaneous execution will improve the execution speed of complicated FOC algorithm and hence the dynamic performance of the drives. This is also the main reason that the latest DSP development kit such as F2812 eZdsp had adopted FPGA chip as co-processor to speed up the execution. Moreover, due to the hardware reconfigurable FPGA feature and the modularity presented in FOCIC, the system can be easily adopted to control four-phase or six-phase induction motors.

2 Principle of Field-Oriented Control

Field-Oriented Control (FOC) is first proposed by Blaschke [10] in 1972 to develop high performance speed and torque control for an induction motor. Since then a large number of technical papers [11] appears in the literature to improve the implementation and performance of FOC of induction machine. The principle of FOC [12] is based on the control of flux component, I_{ds} and the torque component, I_{qs} of the stator current in order to control an AC induction motor like a separated excited DC machine. These two components are the dc values in synchronous rotating frame that is converted to a stationary frame with the help of a unit vector ($\cos \theta_e$ and $\sin \theta_e$) generated from the flux vector signals ψ_{dr}^s and ψ_{qr}^s . The resulting stationary frame signals are then feed to the PI controller to convert to phase voltage commands for voltage source inverter. These conversion processes involve complex mathematical computation and hence high speed processor is needed. The FOCIC IC developed in this project able to solve this problem as the total computation time is only few microseconds due to its capability of executing several processes simultaneously instead of executing the instruction in sequential manner.

3 System design of the FOCIC IC

3 Phase AC induction motors have been the major workhouses in industrial for variable-speed application [12]. A new control structure is developed in this paper for the digital realization of field oriented controlled induction motor. Fig 1 shows the configuration of the FOCIC control IC of a 3-phase induction motor. The principle of FOC is based on the control of flux component, I_d and the torque component, I_q of the stator current in order to control an AC induction motor like a separated excited DC machine.

The machine terminal phase current, I_a and I_b are converted to I_α and I_β components by Clarke transformation with Eqn 1 and Eqn 2.

$$I_\alpha = I_a \quad (1)$$

$$I_\beta = (2I_b + I_a) / \sqrt{3} \quad (2)$$

These are then converted to synchronously rotating frame, I_d and I_q by the unit vectors, $\sin \theta$ and $\cos \theta$ with Park transformation, using Eqn 3 and Eqn 4.

$$I_d = I_\alpha \cos \theta + I_\beta \sin \theta \quad (3)$$

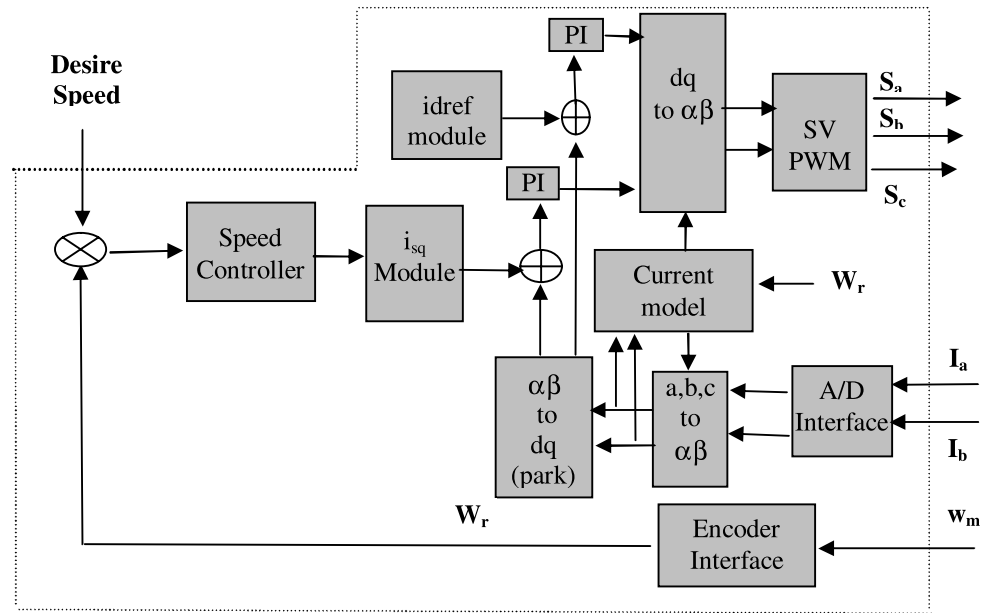


Fig. 1. Control block diagram of the FOCIM.

$$I_q = -I_\alpha \sin \theta + I_\beta \cos \theta \quad (4)$$

The unit vectors, $\sin \theta$ and $\cos \theta$ are very crucial in correct alignment of I_d with the flux vector, ψ_r and I_q perpendicular to it. The unit vectors are generated by the current model based on I_α , I_β and ω_r by implementing Eqn 5 to Eqn 9.

$$\sin \theta = \psi_{qr} / \psi_r \quad (5)$$

$$\cos \theta = \psi_{dr} / \psi_r \quad (6)$$

$$\text{Where } \psi_r = \sqrt{\psi_{qr}^2 + \psi_{dr}^2} \quad (7)$$

$$\text{and } \psi_{dr_{k+1}} = \frac{L_m}{T_r} I_\alpha - \omega_r \psi_{qr_k} - \frac{1}{T_r} \psi_{dr_k} \quad (8)$$

$$\psi_{qr_{k+1}} = \frac{L_m}{T_r} I_\beta + \omega_r \psi_{dr_k} - \frac{1}{T_r} \psi_{qr_k} \quad (9)$$

Where θ is the rotor flux position, L_m is magnetizing inductance, T_r is the rotor circuit time constant and ω_r is the feedback speed.

The command value of I_{sdref} is obtained from the Idref module with Eqn 10.

$$I_{sdref} = (\text{Phir}^*) * L_m \quad (10)$$

Where Phir^* is set to 0.95.

The I_{sqref} is obtained from the PI velocity controller module by implementing Eqn 11.

$$I_{sqref} = (2/3) * (p/4) * (L_r/L_m) * (T_e^*/\text{Phir}) \quad (11)$$

$$\text{Where } \text{Phir} = L_m * I_d / (1 + T_r) \quad (12)$$

L_m = magnetizing inductance, T_r = rotor time, i.e L_r/R_r , L_r = rotor inductance, R_r = rotor resistance, p = no of pole inside the induction motor.

The torque reference, T_e^* is obtained by comparing the desired speed with the motor's feedback speed via PI controller. The parameters employed in this project are shown in Table I.

In order to simplify the hardware setup to verify the functionality of the IC, the reference speed is preset using constant value. A clock divider is included in the design to adjust the input clock frequency (100 MHz) to the desired sampling frequency, f_{sampling} of the feedback current, I_a and I_b . In this case, the input clock frequency, 100 MHz is divided into 1750 Hz, which is the clock input to the Clarke Module to sample the current, I_a and I_b . That means, if the frequency of the current I_a and I_b is 50 Hz, about 35 samples per cycle would be captured for further analysis. The simulation has shown that the space vector modulation, SVM gate signals, T_a , T_b , T_c and their complementary signals is changing from sector 6 – 1 – 2 – 3 etc. The correct sequence of the signals is very much depends on the sampling rate of I_a and I_b . The sampling rate can be determined by Eqn 13.

$$f_{\text{sampling}} = \text{Total no of samples} / T \quad (13)$$

where T is the fundamental period of I_a and I_b . Hence the inverter gate's switching frequency is given in Eqn 14.

$$f_{\text{switching}} = (f_{\text{sampling}} / 2) * n, \quad (14)$$

where n is integer 1, 2, etc.

The overall design is downloaded to Altera UP3 Board and is tested with the three phase bridge inverter to drive a single cage three phase Y connected AC induction motor.

Table I. The rated value and the parameters.

Rated power P_n	1 KW
Rated voltage, V_n	415 V
Rated current, I_n	1.5 A
Rated speed	1500 rpm
Magnetizing inductance (L_m)	34.7 mH
Rotor inductance (L_r)	35.5mH
Rotor resistance (R_r)	0.228

4 Simulation and experimental result

The simulation result of the overall system is shown in Fig 2(a). The sampling frequency is about 1750 Hz as indicated as clock in the waveform. The switching signal, denoted as T_{aout} , T_{bout} and T_{cout} is changing from sector 5 – 2 – 1 – 6 – 5 etc. Fig 2(b) shows the experimental result of the 3-phase bridge inverter gate signals, S_a , S_b and S_c that change from sector 4 to sector 5. As shown in Fig 2(b), the switching frequency is about 7.692 KHz, (i.e. $130 \mu s$), which confirms the switching time, T_s preset inside FOCIC. These

gate signals are used to switch the 3-phase bridge inverter in order to convert a 200 V_{dc} into a 50 Hz, 3-phase AC voltage (i.e. V_a, V_b and V_c) which will drive a 1 KW induction motor.

The terminal voltage of Va-Vb measured by using differential probe and the terminal current waveform by current probe is recorded in Fig. 2 (c). The frequency of terminal current obtained is about 49.18 Hz, which is very close to the 50 Hz as specified in the FOCIC.

The comparison of the desired speed and the feedback speed is shown in Fig 2 (d). The feedback speed is measured by using a digital tachometer from Onosokki and send to PC via DAQ card. The initial speed is set to 80rad/s (or 764rpm) and step up to 100rad/s (955rpm) at $t = 2$ s. As shown in Fig. 2 (d) the feedback speed able to achieve 80rad/s and stabilise after 0.9s. Also the system able to response to the step change at $t = 2$ s and stabilise at 100 rad/s. However the error between the desired speed and feedback speed during start up and step change can be further improved by fine-tuning the PI controller before incorporated into the FPGA chip. In addition, the accuracy of the flux estimator also plays a major role in the performance and accuracy of the controller.

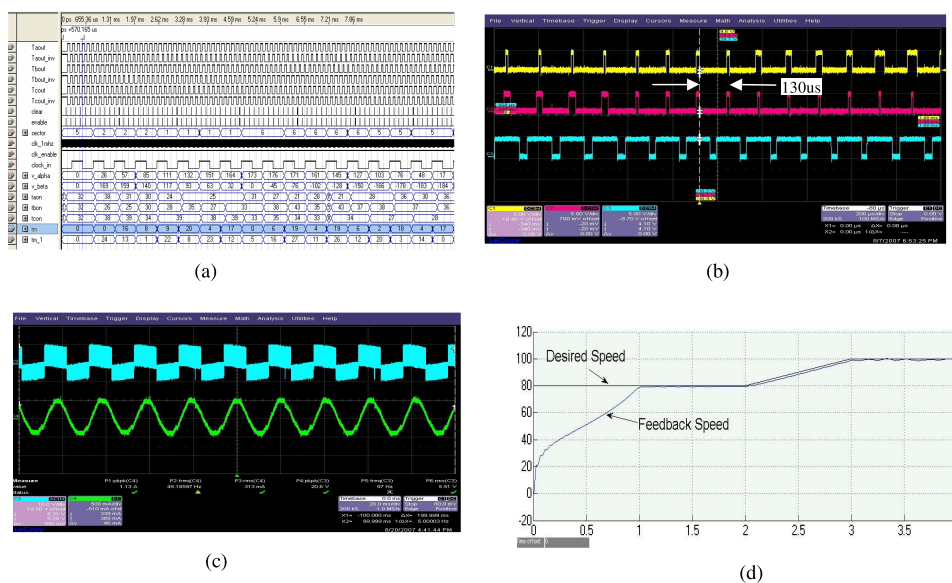


Fig. 2. (a) Simulation result of FOCIC.
 (b) The Experimental result of Sa, Sb and Sc from sector 4 to sector 5.
 (c) The experimental result of Va, Vb and Va-Vb.
 (d) The desired speed vs, feedback speed.

5 Conclusion

This paper presents a complete realization of integrated SVM and FOC, in a single FPGA chip, FOCIC. The developed FOCIC IC can be incorporated with general purpose ADC or micro-controller to obtain the feedback current and hence generate the SVM switching signal to drive IGBTs based inverter.

The FOCIC able to generate a switching signal that up to 40 kHz in order to reduce the acoustic noise by just changing the f_{sampling} value in the design. The overall design able to produce a low cost solution for high performance 3-phase induction motor drives system due to the fact that a FPGA chip is a blank IC chip without any pre-built peripherals like others micro-controller chip. Moreover, the hardware re-configurable feature and the modularity in FOCIC also enable it to be adopted to control four phase or six-phase induction motors. In addition, the simultaneous execution feature enables fast execution speed open up the potential to implement complex arithmetic algorithm such as artificial intelligent based rotor flux estimator to replace the current model for better speed response.