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Negative charge pump circuit with large output current and high power efficiency

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Abstract: In this paper, we propose a new negative charge pump circuit which is based on the Dickson circuit. This circuit overcomes the limitation of the conventional Dickson pump circuit and doubler-based one such as large loss in output voltage, low power efficiency, and small output current. Comparing the new one with the conventional doubler-based circuit at the $V_{DD} = 8\,V$ indicates the pumping time faster by 83.8%, 7 times larger output current, power efficiency better by 23.1%, and the layout area smaller by 15%. We have verified the new pump circuit using the commercial CMOS process with high-voltage devices.

Keywords: negative charge pump circuit, high power efficiency, large output current, low voltage

Classification: Integrated circuits

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1 Introduction

Negative charge pumps which can deliver a negative voltage lower than the ground potential (V_{SS}) from its supply voltage (V_{DD}) have been widely used

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in many analog and memory circuits such as Light-Emitting Display (LED) driver ICs, image-sensor driver ICs, DRAMs, FLASH memories and so on. A negative voltage can be generated by using the voltage-doubler-based negative charge pump circuit [1] or the Dickson-based one [2]. In some cases, a voltage lower than $-V_{DD}$ is needed and this can be easily implemented by cascading single-stage pump circuit more than one. Multiple stages of pump circuit can lead their devices to suffer voltage stress higher than the V_{DD}. Hence most charge pumps need high-voltage devices are able to tolerate voltage stress higher than the V_{DD}. Taking an example, the process used in this paper supports the high-voltage NMOS and PMOS devices which can function well up to as high as 40 V in addition to its normal $5-$ V PMOS and NMOS devices. The cross-sectional view of these high-voltage NMOS and PMOS devices is shown in Figure 1 (a), where high-voltage NMOS is made on the isolated P-well being surrounded by the Deep-N-well (DNW). And, high-voltage PMOS is put on the N-well and beneath this N-well, the DNW surrounds it. This cross-sectional structure for high-voltage PMOS and NMOS devices is obtained from industry and can be thought as a typical structure which can be applied to most of fabrication processes with high-voltage devices.

Now let us take a closer look on the conventional doubler-based negative pump in Figure 1 (b). Here the Cn's are pumping capacitors and the MNn's

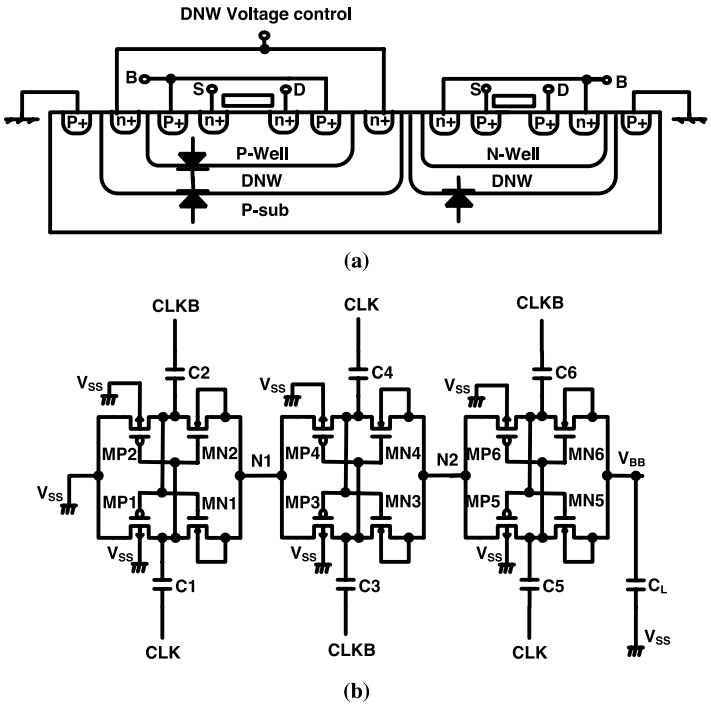

Fig. 1. (a) A cross-sectional view of the $40-$ V NMOS and PMOS devices. Here the DNW means the Deep-N-Well and the diode symbol represents the back-to-back diode. (b) A schematic of the conventional doubler-based negative charge pump circuit

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and MPn's are NMOS and PMOS switches, respectively. The C_L is the load capacitor and the CLK and CLKB are the non-overlapping clocks. In Figure 1 (b), the PMOS bulk terminal tied to the V_{SS} can raise absolute value of its threshold voltage because its source voltage becomes lower thereby the output voltage (V_{BB}) in Figure 1 (b) being degraded due to this body effect of MPn's becoming more severe. In the other way, if the bulk is tied to its own source terminal, it can form a forward-biased diode between the N-well and the P-substrate thus introducing a severe latch-up problem. To avoid this phenomenon, all the PMOS devices in Figure 1 (b) should have their bulks tied to the V_{SS} instead of being tied to their own source terminals thereby suffering severe body effect. One more concern about the circuit in Figure 1 (b) is the number of pumping capacitors. The cross-coupled nature of Figure 1 (b) needs twice more capacitors than the Dickson-based circuit and this can be a burden in terms of manufacturing cost when the pumping capacitors can not be made inside a chip because of its capacitance values being so much large.

To avoid suffering body effect and reduce the number of pumping capacitors, we will take an approach based on the Dickson circuit in developing new negative charge pump in this paper. Though many positive charge pump circuits have been developed based on the Dickson circuit [3, 4], they can not be used as a negative charge pump circuit only by simply replacing PMOS with NMOS and NMOS with PMOS.

2 Proposed negative charge pump

A new negative charge pump circuit is proposed in Figure 2 (a). Here, the MT1, MT2, MT3, and MT4 act as transfer switches that are made of NMOS and deliver their generated negative voltages to the following stages. The C1, C2, and C3 are pumping capacitors. When the CLKB and CLK are low and high, respectively, the MP1 being turned on by the CLKB applies the V_{DD} on the gate of the MT1 thereby the MT1 being turned on, too. At this moment, because the CLK is high and the N1 is connected to the V_{SS} through the MT1, a voltage as low as $-V_{DD}$ is stored across the C1. At the same time, we can see the following stage where the MP2 is turned off by the CLK but the MN2 is on. The MN2 being on makes the MT2 off thus the N2 being able to fall down to $-2\,V_{DD}$ by the CLKB going low without losing any charges backward to the N1. And, this N2 node as low as $-2\,V_{DD}$ is connected to the following N3 node because of the MT3 being turned on by the CLKB being low.

At the next phase, when the CLKB and CLK are high and low, respectively, the MN1 and MP1 in Figure 2 (a) are turned on and off, respectively. Thus, the MT1 becomes turned off allowing the N1 node to be as low as $-V_{DD}$. This N1 voltage as low as $-V_{DD}$ can be transferred to the following N2 node through the MT2 being on at this moment. When the CLK is low, the MP2 is turned on thereby the MT2 being on, too. Similarly, the MT3 is off and the MT4 is on. The MT4 in the final stage in Figure 2 (b) delivers the N3

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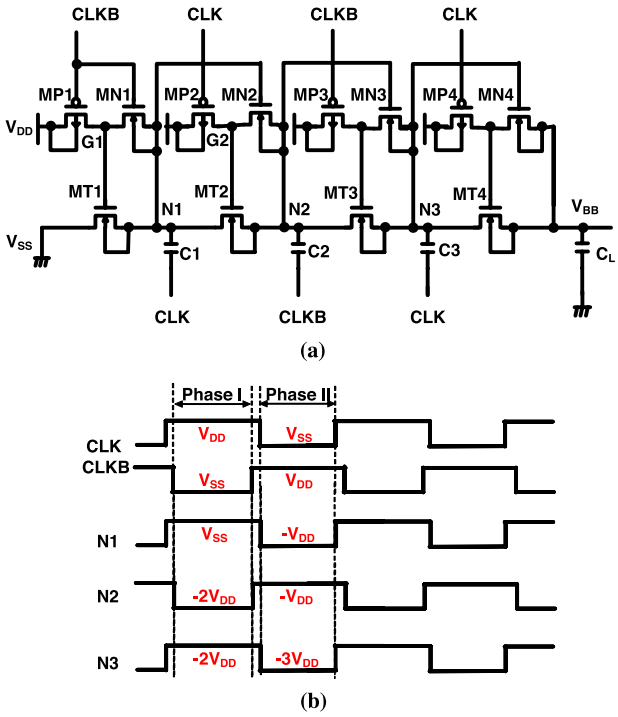

Fig. 2. (a) A schematic of the proposed negative charge pump circuit (b) Non-overlapping clock signals and node voltages

voltage as low as $-3\,V_{DD}$ to the V_{BB}. Of course, at this time, the N3 voltage can not be transferred backward to the N2 because of the MT3 being off.

Here it should be noted that all the transfer switches of the MT1, MT2, MT3, and MT4 are turned on by the V_{DD} through their own PMOS switches of the MP1, MP2, MP3, and MP4, respectively. This gate voltage of the transfer switch as high as the V_{DD} increase the conductance of the transfer switches thereby delivering larger output current than the circuit in Figure 1 (b). If we look at the MT4, its gate-source voltage reaches as high $4\,V_{DD}$ thus being able to achieve large output current even though the V_{DD} is very low.

One more thing to comment here is that the NMOS transfer switches in the proposed circuit do not suffer any body effect like the PMOS transfer switches of the doubler-based circuit shown in Figure 1 (b). As you can see Figure 2 (a), the transfer switches are made of NMOS and their bulks are connected to their own sources thereby the threshold voltage not being degraded at all. These transfer switches with their own sources and bulks tided together do not introduce a latch-up related issue because of the DNW biased by the V_{DD} and the bulk of NMOS biased negatively not forming any forward-biased diode.

Figure 2 (b) shows non-overlapping clocks of the CLK and CLKB used in Figures 1 (b) and 2 (a). Here the CLK and CLKB are not allowed to be low simultaneously. If both the CLK and CLKB are low simultaneously, the pumping voltages which are lowered below the V_{SS} may be transferred backward to the V_{SS} instead of being transferred forward to the output. For example, when the CLK and CLKB are simultaneously low, a negative

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voltage on the N1 can be lost into the V_{SS} partly. To avoid this voltage loss, the CLK and CLKB which are not low simultaneously are generated by the non-overlapping clock generator circuit. Because the non-overlapping clock circuit is very general and easily can be implemented [5], we do not explain it in more detail in this paper.

3 Simulation

The simulation is done by HSPICE using a high-voltage CMOS process with a minimum channel length as long as 3.5 μm and a maximum voltage as high as 40 V. The SPICE parameters are obtained from industry so their values are thought to be very practical. First of all, we compared which circuit can decrease its output voltage faster than the other between the charge pump circuits of Figures 1 (b) and 2 (a). Figures 3 (a) and (b) are for the $V_{DD} = 8$ V and $V_{DD} = 3.3$ V, respectively. As you can see from these figures the proposed circuit lowers its output voltage much faster, because the transfer switches in Figure 2 (a) have much larger conductance than the conventional circuit thus delivering pumping current more to the load. If we define the pumping time as a time needed for its output voltage to be lowered as low as 90% of $-3\,V_{DD}$, the pumping time of the proposed circuit is faster than the conventional by as much as 83.8%, as shown in Figure 3 (a). For the Figure 3 (b), this comparison is done again with the $V_{DD} = 3.3$ V. Here the

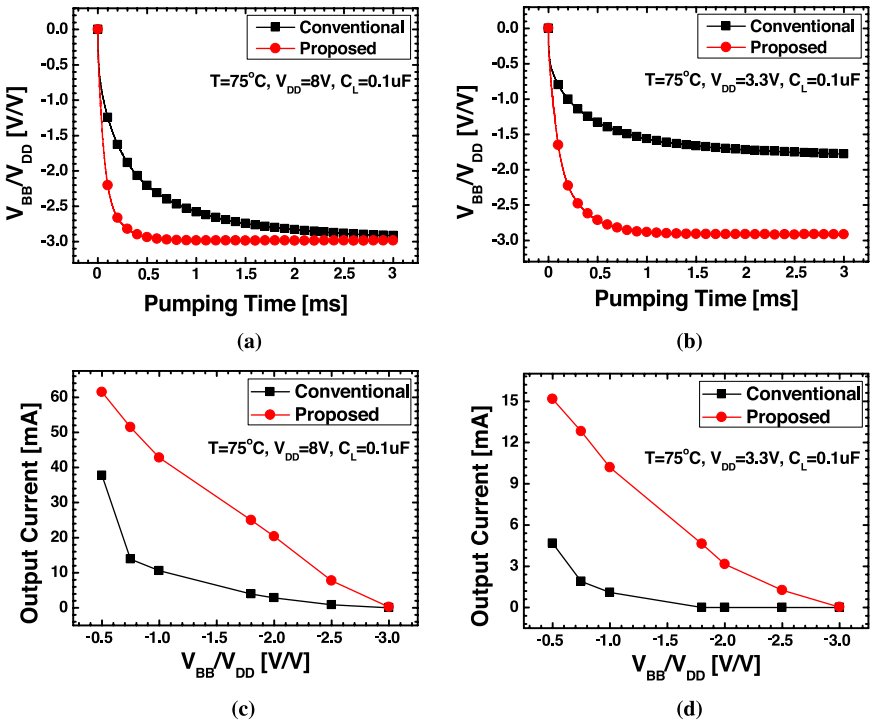

Fig. 3. Comparison of the pumping time between the conventional pump circuit and the proposed one (a) at the $V_{DD} = 8$ V and (b) at the $V_{DD} = 3.3$ V Comparison of the output current (c) at the $V_{DD} = 8$ V and (d) at the $V_{DD} = 3.3$ V

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pumping time of Figure 2 (a) is observed by 0.48 ms, while the conventional circuit can not decrease down to $-3\,V_{DD}$ but saturates around $-1.8\,V_{DD}$. This is because the PMOS transfer switches in Figure 1 (b) suffer severe body effect thus they losing their generated voltages in delivering them to the following stages.

Figures 3 (c) and (d) compare how much output current they can deliver to the load when the $V_{DD} = 8\,V$ and $V_{DD} = 3.3\,V$, respectively. When the $V_{BB}/V_{DD} = -1$ and the $V_{DD} = 8\,V$, the conventional doubler-based circuit and the proposed Dickson-based circuit can deliver 10.57 mA and 42.75 mA to the load, respectively. If we decrease the V_{BB}/V_{DD} down to -2, the output current of Figure 1 (b) is as small as 2.85 mA while that of Figure 2 (a) reaches as large as 20.32 mA. Similarly, when the V_{DD} is 3.3 V, we also plotted in Figure 3 (d) how much current is delivered to the load with varying the V_{BB}/V_{DD}. When the $V_{BB}/V_{DD} = -1$, the conventional and the proposed circuit can deliver 1.09 mA and 10.19 mA, respectively. When the $V_{BB}/V_{DD} = -2$, they deliver 0 A and 3.15 mA, respectively. As you can see in Figures 3 (c) and (d), the gap in output current increases sharply with the V_{BB}/V_{DD} increasing from -3 to -1.

Finally, comparing power efficiency between the conventional and proposed circuits indicates the power efficiency of the proposed circuit is better than the doubler-based circuit in Figure 1 (b) by as much as 23.1% when V_{DD} =8 V and the $V_{BB}/V_{DD} = -2$. And, when the $V_{DD} = 3.3\,V$ and the $V_{BB}/V_{DD} = -1.5$, the efficiency of the proposed circuit seems to be better by 37.8% than the circuit in Figure 1 (b). Here it should be noted that the power efficiency of the proposed circuit is much better than the conventional doubler-based circuit over the whole range of V_{BB}/V_{DD}. For the layout area, the proposed circuit occupies layout area less by 15% than the conventional in this high-voltage CMOS design rules.

4 Conclusion

The new negative charge pump circuit based on the Dickson circuit was proposed in this paper. Unlike the doubler-based circuit, this circuit does not have any cross-coupled architecture thereby minimizing the number of pumping capacitors. And, the transfer switch controlled by large gate-drive voltage can deliver large output current to the load. Moreover, using only NMOS transfer switch and not using PMOS one can avoid any degradation of the threshold voltage caused by the body effect. The new circuit has been verified in the commercial high-voltage CMOS process that shows faster pumping speed, larger output current, better power efficiency, and less layout area than the conventional in the whole range of V_{BB}/V_{DD}.

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