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A UWB LNA with interference rejection using enhanced-Q active inductor

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Abstract: This paper presents a new technique for improving the quality factor of conventional active inductors by using the drain-source capacitance of a MOSFET in the cut-off region. This inductor is utilized to design a tunable notch filter for interference rejection in UWB LNA. Using a 0.13 μm CMOS technology, simulation shows that the notch frequency can be tuned for about 1 GHz frequency range, and the quality factor is improved more than one order of magnitude compared to conventional active inductor. The power dissipation of the new active inductor is 2.4 mW from 1.2 V supply.

Keywords: LNA, active inductor, image rejection, notch filter, tunable notch, UWB

Classification: Integrated circuits

References

[1] C.-C. Wei, H.-C. Chiu, and W.-S. Feng "An Ultra-Wideband CMOS VCO with 3-5 GHz Tuning Range," *IEEE International Workshop on Radio-Frequency Integration Technology,* Nov. 30–Dec. 02, 2005.

[2] C.-C. Hsiao, C.-W. Kuo, C.-C. Ho, and Y.-J. Chan, "Improved Quality-Factor of 0.18-μm CMOS Active Inductor by a Feedback Resistance Design," *IEEE Microw. Wireless Compon. Lett.*, vol. 12, no. 12, Dec. 2002.

[3] T. Y. K. Lin and A. J. Payne, "Design of a Low-Voltage, Low-Power, Wide-Tuning Integrated Oscillator," *IEEE International Symposium Circuits Syst.*, May 28–31, 2000.

[4] M. Mehrabian and A. Nabavi, "An Ultra Wide Tuning Range VCO with Active Tunable Inductors," International Review of Electrical Engineering - Aug. 2008.

[5] R. Akbari-Dilmaghani, A. Payne, and C. Toumazou, "A High Q RF' CMOS Differential Active Inductor," *IEEE International Conference Circuits Syst.*, vol. 3, pp. 157–160, 1998.

[6] R. Mukhopadhyay, P. Sen, N. Srirattana, J. Lee, C.-H. Lee, S. Nuttinck, A. Joseph, J. D. Cressler, and J. Laskar, "Reconfigurable RFICs in Si-Based Technologies for a Compact Intelligent RF Front-End," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, Jan. 2005.

[7] H. Elahi, "Design of Low Noise Amplifier for Ultra Wide Band Systems," Master Thesis, Tarbiat Modares University, July 2008.

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1 Introduction

The function of an UWB device can be seriously affected by interference from other wireless protocols, namely “in-band” interference. To suppress the interference frequencies, a notch filter, consisting of series inductor and capacitance, can be utilized in LNA structure. The desired frequency in notch filter is given by:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

Where L is the inductance and C is the capacitance in the filter.

On-chip spiral inductors often need large silicon area. Moreover, due to resistive loss and capacitive coupling to substrate, their inductance and quality factor are lower than that required for most applications. In order to overcome these limitations, active inductors have been proposed [1, 3, 5], which provide high quality factors, small chip areas, and tunable features.

In this paper, we show that the quality factor of conventional active inductor is improved by using the drain-source capacitance of a MOSFET biased in the cut-off region. Simulation results are given to illustrate the use of the new inductor for designing tunable notch filters suited for interference rejection in UWB LNA.

2 Active inductor design

Active inductor can be realized by connecting two transconductors with resistive feedback topology, as shown in Fig. 1 (a) [1, 3, 5]. In this figure, transistor M_2 is employed to reduce the output conductance (g_{ds}) [1, 2, 3, 4, 5], which enhances the inductance, quality factor, and frequency tuning ranges [1]. Also, a feedback resistance R_f between M_1 and M_3 can significantly increase the inductance of cascode-grounded active inductor [2]. The equivalent circuit model of the active inductor is shown in Fig. 1 (b).

The active inductor in Fig. 1 (c) exploits a tunable feedback resistance [1, 6], implemented by a passive poly resistor ($\mathrm{R_f}$) in parallel with $\mathrm{M_4}$. The gate-source voltage ($\mathrm{V_{tune}}$) controls the total effective resistance ($\mathrm{R_{eff}}$).

In this paper, the active resistor has been implemented using a 0.13 μm CMOS technology. A tunable resistance from 100 Ω to 1.6 kΩ has been achieved for $\mathrm{V_{tune}} = 1.2$ V to $\mathrm{V_{tune}} = .4$ V, as illustrated in Fig. 1 (d).

By tuning the effective resistance, we control both the inductance value and the quality factor. It is required to compensate for the fall in quality-factor due to increase in effective resistance, which requires a secondary control parameter. This is accomplished by changing g_{ds} with the help of V_c. Thus, the required inductance and quality factor at frequency of operation (f_Q) is achieved by controlling V_{tune} and V_c simultaneously [1].

For further enhancement of quality factor and inductance, we utilize the transistor $\mathrm{M_5}$ in parallel with feedback resistance R_f, as shown in Fig. 1 (e). This transistor, which operates in the cut-off region, exhibits a frequency dependent capacitance as shown in Fig. 1 (f).

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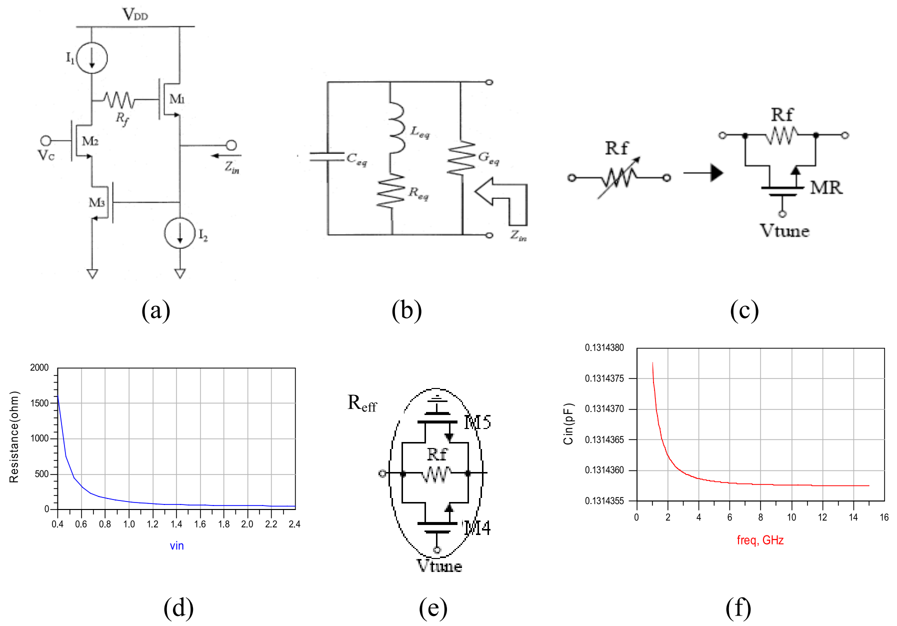

Fig. 1. (a) Schematic of cascode-grounded active inductor with a feedback resistance (b) Equivalent circuit model of active inductor (c) Tunable active resistor topology (d) Variation of resistance for different tuning voltages (e) Proposed active resistance with parallel MOSFET (f) Variation of capacitance in proposed active resistance versus frequency.

The values of each component of equivalent circuit model are expressed below (Cp is equivalent capacitance of M_5):

$$C_{eq} = C_{gs3} - \frac{2\omega C_p R_{eff} g_{ds2} (R_{eff} g_{ds2} + 1) - R_{eff} \omega C_p (R_{eff} g_{ds2}^2 + 2g_{ds2})}{(R_{eff} g_{ds2} + 1)^2 + \omega^2 C_p^2 R_{eff}^2} \tag{2}$$

$$G_{eq} = \frac{2\omega^2 C_p^2 R_{eff}^2 g_{ds2} + (R_{eff} g_{ds2} + 1)(R_{eff} g_{ds2}^2 + 2g_{ds2})}{(R_{eff} g_{ds2} + 1)^2 + \omega^2 C_p^2 R_{eff}^2} \tag{3}$$

$$R_{eq} = \frac{g_{m1} g_{ds2} g_{ds3} + \omega^2 \left[g_{m2} C_{gs1}^2 + (C_{gs1} C_{gs2}) \left[\frac{g_{m1} C_p C_{gs1} R_{eff}^2 g_{ds2}}{1+\omega^2 C_p^2 R_{eff}^2} - g_{m1} \left(1 + \frac{R_{eff} g_{ds2}}{1+\omega^2 C_p^2 R_{eff}^2} \right) \right] \right]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{4}$$

$$L_{eq} = \frac{g_{m1} g_{m2} C_{gs1} + \omega^2 (C_{gs1} C_{gs2}) \left[\frac{g_{m1} C_p R_{eff}^2 g_{ds2}}{1+\omega^2 C_p^2 R_{eff}^2} + g_{m1} C_{gs1} \left(1 + \frac{R_{eff} g_{ds2}}{1+\omega^2 C_p^2 R_{eff}^2} \right) \right]}{g_{m1}^2 g_{m2} g_{m3} + \omega^2 g_{m2} g_{m3} C_{gs1}^2} \tag{5}$$

In order to have L_{eq} greater and R_{eq} smaller than other conventional inductors, the following relations should be satisfied.

$$C_p > \frac{-g_{ds2}}{\omega^2 C_{gs1}} \tag{6}$$

$$C_p > \frac{C_{gs1} g_{ds2}}{\omega^2} \tag{7}$$

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Eq. (6) is satisfied for all values of C_p, and the capacitance C_p will always increase L_{eq}.

3 LNA with tunable notch

The notch filter, designed with the above active inductor, has been employed within UWB LNA architecture of Fig. 2. This LNA uses resistive shunt-feedback for the first stage and cascade structure for the second stage. The LNA has been designed in a 0.13 μm CMOS process. The power gain of the LNA is 20 dB with 3-dB bandwidth of 3–13 GHz. The input and output matching (S_{11} and S_{22}) are below −10 dB. LNA consumes 12 mW from a 1.2 V supply, whereas the power of the active filter is 2.4 mW [7].

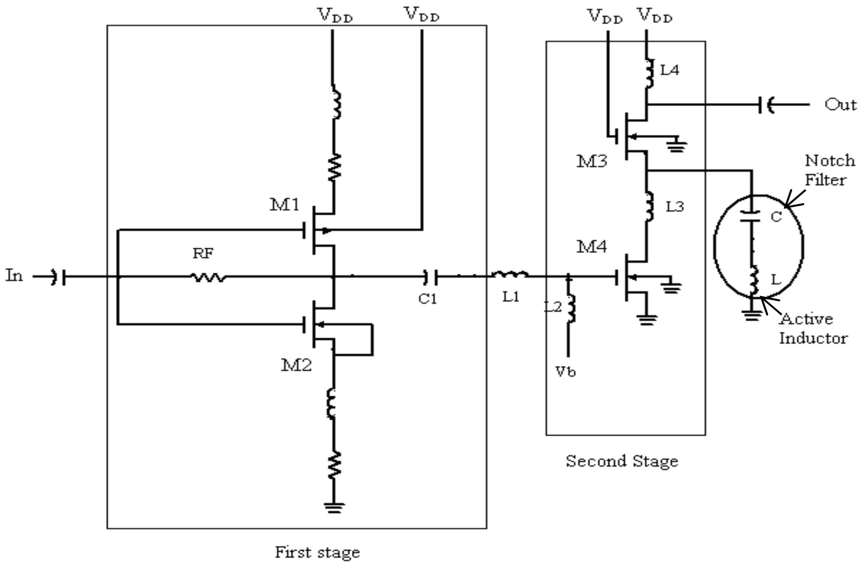

Fig. 2. LNA with tunable notch.

4 Simulation results

Fig. 3 (a, b) and Fig. 3 (c, d) show, respectively, the analytical and simulation results of LNA with tunable notch filter. As shown in these figures, the quality factor of the new active inductor is improved.

Fig. 3 (c) shows S_{21} parameter of LNA with active inductor without C_p. This figure illustrates that in 5∼7 GHz frequency band, the quality factor of active inductor is low. The active inductance is about 0.9 nH and the resistance is about 6.64 Ohm. The Q factor can be expressed as below (by eliminating the effects of C_{eq} and G_{eq}):

$$Q = \frac{2\pi f L}{R} \tag{8}$$

$$\text{For f} = 5.4\,\text{GHz}, \quad \text{L} = .9\,\text{nH} \quad \text{R} = 6.64\,\text{Ohm} \rightarrow \text{Q} = 6$$

Fig. 3 (d) shows S_{21} parameter of LNA with the new active inductor. Obviously, in 4∼6 GHz frequency band the quality factor of active inductor is

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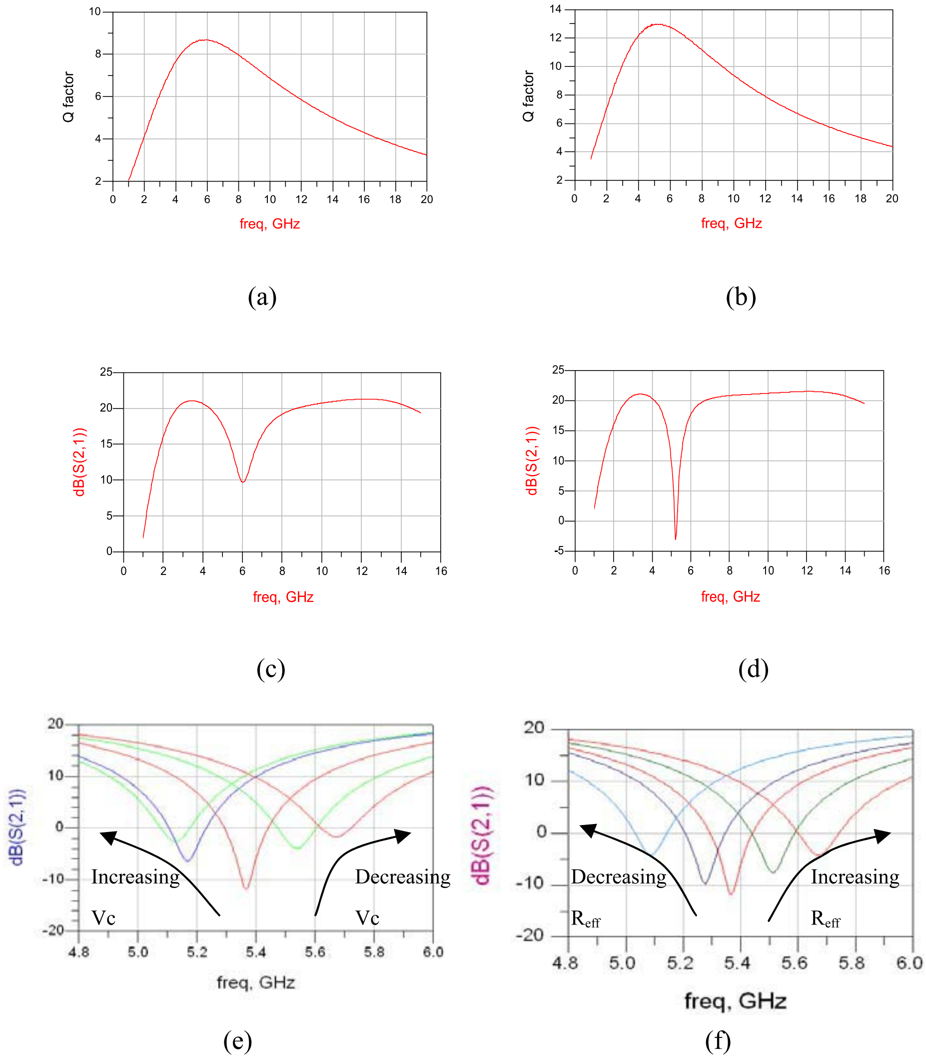

Fig. 3. (a) Q factor of conventional active inductor, (b) Q factor of new active inductor, (c) S_{21} parameter with conventional active inductor, (d) S_{21} parameter with new active inductor (e) Controlling notch frequency by V_c (f) S_{21} parameter by controlling V_{tune}.

improved, while the inductance is increased about 1.5 nH. The resistance is decreased to about 0.24 Ohm. The Q factor by using (8) and neglecting the effects of C_{eq} and G_{eq} can be expressed as follows.

$$f = 5.4\,\mathrm{GHz} \quad L = 1.2\,\mathrm{nH} \quad R = 0.24\,\mathrm{Ohm} \rightarrow Q = 170$$

By changing V_{tune} and V_c, we control the inductance of active inductor, tuning the notch frequency from 5 to 6 GHz. Fig. 3 (e) and Fig. 3 (f) show the variations of notch frequency for different tuning voltages.

To have proper parameters for the active inductor to make a notch filter at the frequency f_0 ($\omega_0 = 2\pi f_0$) one may use the following formulas:

$$Z_{in} = R_{in} + jX_{in} = \left(\frac{1}{j\omega C_{eq}} || \frac{1}{R_{eq} + j\omega L_{eq}} || G_{eq}\right) \tag{9}$$

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$$Q = \frac{X_{in}}{R_{in}} = \frac{\omega_0 \left(L_{eq} - G_{eq}R_{eq}^2 - \omega_0^2 L_{eq}^2 C_{eq}\right)}{R_{eq} + G_{eq}R_{eq}^2 + \omega_0^2 L_{eq}^2 G_{eq}} \tag{10}$$

$$\frac{dQ}{d\omega}|_{\omega=\omega 0} = 0 \tag{11}$$

On the other hand, to have maximum G_{eq}, C_{eq}, L_{eq} and minimum R_{eq}, the following equations should be satisfied:

$$\frac{dG_{eq}}{d\omega}|_{\omega=\omega 0} = 0 \tag{12}$$

$$\frac{dC_{eq}}{d\omega}|_{\omega=\omega 0} = 0 \tag{13}$$

$$\frac{dL_{eq}}{d\omega}|_{\omega=\omega 0} = 0 \tag{14}$$

$$\frac{dR_{eq}}{d\omega}|_{\omega=\omega 0} = 0 \tag{15}$$

Therefore, by choosing proper L_{eq} from Eq. (11)-(15), we can determine the value of the series passive capacitance C (Fig. 2) from Eq. (1). Note that by changing the controlling voltages the quality factor will decrease.

5 Conclusion

This paper presented a new technique for improving the quality factor in conventional active inductor, by exploiting the drain-source capacitance of a MOSFET biased in the cut-off region. The new active inductor is utilized to implement tunable notch filter for UWB LNA, providing high interference rejection capability for about 1 GHz frequency range. Simulation results with a 0.13 μm CMOS technology illustrate interference rejection by more than 45 dB. Also, the inductor consumes 2.4 mW from 1.2 V supply.

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