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Novel First-one detector architecture applied in VLC

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Abstract: The variable length coding (VLC) has gained greater attention due to its wide application in the international standard, H.264/AVC and Chinese standard, AVS. A First-one detector is an indispensable module of VLC, such as CAVLC and Exp-Golomb coding. In this paper, a novel First-one implementation architecture is proposed, which can locate the First-one in the codeword in only one cycle. The architecture applies the combinational logic to parse the position of the separator '1'. Compared with the conventional methods, this approach has higher efficiency.

Keywords: VLSI architecture, variable length coding, combination logical

Classification: Integrated circuits

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1 Introduction

The international standard JVT and the Chinese audio/video standard AVS apply the Exp-Golomb coding methods and Context-based adaptive variable length coding (CAVLC) to solve the entropy- coding problem. Therefore, the

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design of the CAVLC and Exp-Golomb encoder and decoder is significant. As to the implementation of the VLC decoder (VLD), several special-purpose VLSI architectures have been proposed in recent years. Among all the architectures, First-One Detector is an indispensable module. There are three kinds of ways to implement the First-One detector. The first is a bit-by-bit detector. The approach costs a lot of unpredictable time (depending on the length of code word) and is unsuitable for real-time application. The second adopts lookup-table method. The method will consume more memory to save the looking up tables. The third is based on combination of series and concurrent to improve hardware decoding. The approach requires additional hardware resources, and its performance is not very good when the length of code word is more than 8 bits. The paper proposed a novel First-one detector architecture to implement the First-one detector in only one cycle with less hardware resource.

2 Problem formation

The VLC codeword consists of prefix and suffix. The number of code words grows exponentially with the length of the suffix. For example, an Exp-Golomb Code is constructed as following,

$$\overbrace{0\ldots01}^{m}\ \overbrace{x_{n-1}x_{n-2}\ldots x_0}^{n}$$

The prefix bits consist of m leading “0’s” and a “1”, where $m \geq 0$ The last n-bit field is the suffix that carries information. Therefore, it is very important to detect the MSB 1 to Exp-Golomb encoder and decoder. Similarly, it will be used in CAVLC decoder.

3 Proposed first-one detector using combinational logical

If there is a VLC codeword x, calculate the following formula:

$$F = x\&(-x) \tag{1}$$

Herein $-x$ denotes the complementary code of x. For example, x=10010111100, then F=000000000100 in term of formula (1). The position of 1 is just the index of the First-One.

In additional, we present the other two methods to look for the First-One, in terms of formula (2) and formula (3).

$$\sim x\&(x-1) \tag{2}$$

$$\sim (x| -x) \tag{3}$$

In prefix-suffix decoding, we must detect the position of the highest order bit “1”. So when the bit stream is input, we make the data reversed and detect the position of the separator “1” by using formula (1). Moreover, the method of reversing the input data is a very simple in hardware implementation, which connects reversely the line of register from high to low.

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4 Simulations and analysis

To compare with the other methods, we assume that the input data length is 32. The decoding time in the bit-by-bit detector will increase in proportional to the length of code word. However, in our approach it only spends one cycle on determine the position of the separator "1", indepently with the length of the input data. This method greatly enhances the efficiency of decoding. Table I shows the time occupying of the two methods.

Table I. the comparison of two methods

Length N	The clock cycle of read bit by bit	The clock cycle of our method
1	1	1
3	2	1
5	3	1
7	4	1
9	5	1
11	6	1
13	7	1
15	8	1
…	…	**1**

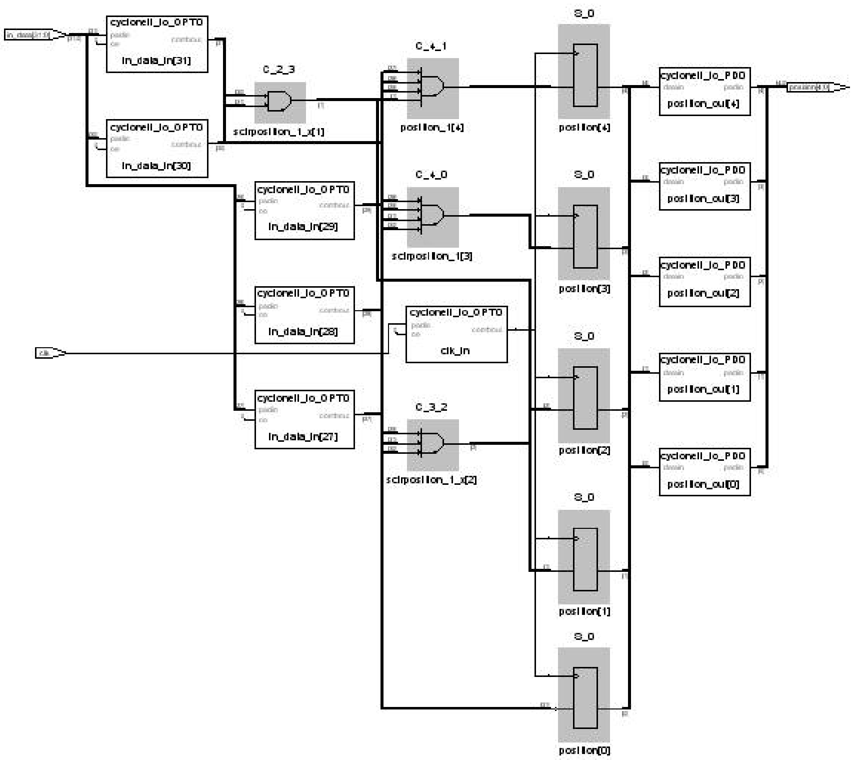

Fig. 1. combinational logical method circuit

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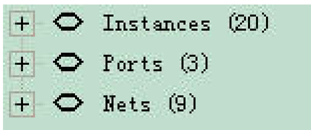

Fig. 2. circuit resource report

The LUT method occupies a lot of RAM/ROM resource in circuit, although it can also solve the problem in only one clock cycle. Take the 1 order Exp-Golomb encoding as an example. If the input code has 32 bits, the output code word may be as long as 63-bit long. The LUT method occupies quite large RAM/ROM, $2^{32} \times 63 = 252\, Gbit$.

Among the proposed 3 different First-one detector as formula (1)-(3), the first method gives the best performance in circuit logic. And the circuit synthesized by Synplify Pro 8.1 is shown in fig. 1. And the circuit resource report is shown in fig. 2.

5 Conclusion

In this paper, we address the problem of First-one detection. The proposed novel approach has capability to easily implement the first-one detection in only one cycle, which is based on combinational logic. The proposed architecture can be employed in many codec, such as Exp-Golomb encoding, CAVLC decoding etc. The future work is to further reduce the resource required.

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