

A Look-ahead Active Body-biasing scheme for SOI-SRAM with dynamic V_{DDM} control

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Abstract: Instability of SRAM memory cells derived from aggressive technology scaling has become one of the most significant issues. Although lowering the supply voltage for a memory cell (V_{DDM}) improves a write margin, which increases the access time. In this paper, we propose a memory cell employing a Look-ahead Active Body-biasing (LAB) scheme for SOI-SRAM with the dynamic V_{DDM} control. Simulation results have shown that the proposed SRAM cell shortens the access time by 54% in the write mode, while expanding read and write margins and reducing effects of variations in the threshold voltage on them.

Keywords: SRAM, V_{DDM} control, SOI, active body-biasing

Classification: Integrated circuits

References

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1 Introduction

In a previous scenario of SRAM development, technology scaling had been

able to achieve the higher performance. However, an unexpected random variation in V_{th} and the lowered supply voltage drastically deteriorate the stability of SRAM memory cells in a sub-100 nm era and beyond. Although lowering the supply voltage for a memory cell (V_{DDM}) expands a write margin [1, 2], it results in degradation of the access time.

In this paper, we propose a Look-ahead Active Body-biasing (LAB) scheme for SOI-SRAM cells with the dynamic V_{DDM} control on PD-SOI, where V_{th} of each transistor can be dynamically controlled thorough the direct body contact [3]. Here, the HTI (Hybrid Trench Isolation) technology, shown in Fig. 1 (a), drastically reduces the area penalty and parasitic gate capacitance to almost the same level as bulk MOSFETs. For SRAM memory cells, the use of bitline signals to control V_{th} of pull-up transistors improves the access time and the read/write margins.

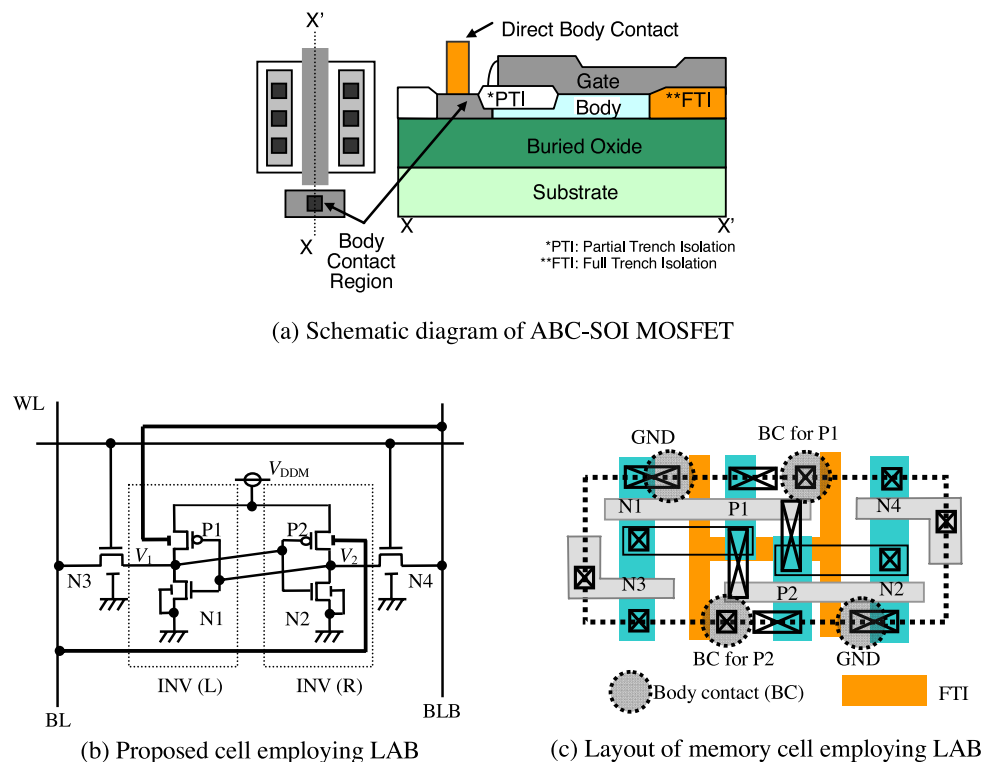


Fig. 1. Proposed SOI-SRAM memory cell.

2 The dynamic V_{DDM} control

Controlling V_{DDM} node in the memory cell improves write and read margins. In the dynamic V_{DDM} control, V_{DDM} is pulled down from V_{DD} ($V_{DDM} < V_{DD}$) in the selected column for write operation, and V_{DDM} is boosted from V_{DD} ($V_{DDM} > V_{DD}$) in the selected column for read operation.

Although lowering V_{DDM} expands a write margin, it results in degradation of the access time. The V_{DDM} control in the read mode improves the discharge current at the data nodes V_1 and V_2 , hence it shorten the read time. On the

other hand, the V_{DDM} control makes the write time longer because the V_{DDM} control pulled down V_{DDM} and degrade the charge current.

3 Look-ahead Active Body-biasing scheme

3.1 Proposed SOI-SRAM

In the proposed SOI-SRAM cell shown in Fig. 1 (b), the bitlines BL and BLB control the bodies of pMOS transistors P2 and P1, respectively.

In case of ‘1’-write operation, for which the voltages of BL and BLB are set to $V_{BL} = V_{DD}$ and $V_{BLB} = 0\text{ V}$, respectively, V_{th} of P1 (V_{th-P1}) is lowered by the forward body-bias $|V_{BS-P1}| = V_{DDM}$, where the body to source voltage $V_{BS-P1} = V_{BLB} - V_{DDM} = -V_{DDM}$. On the other hand, V_{th} of P2 (V_{th-P2}) is lowered by the forward body-bias: $|V_{BS-P2}| = V_{DDM}$ during ‘0’-write operation.

In read operation, for which V_{DDM} is kept higher than V_{DD} and both bitlines BL and BLB are precharged to V_{DD} , both V_{th-P1} and V_{th-P2} are slightly lowered by the forward body-bias: $|V_{BS-P1}| = |V_{BS-P2}| = V_{DDM} - V_{DD}$.

In order to control the body voltage of each transistor, a body contact is required for providing the body-bias. Fig. 1 (c) shows the proposed cell layout of SRAM including the body contacts. Here, all the body contacts are embedded in each memory cell without any additional area.

3.2 Impact of LAB on Access Time and Write/Read Margin

In the proposed SRAM cell based on the LAB scheme, lowering either V_{th-P1} or V_{th-P2} based on the data to be written shortens the write time. For example, in case of the ‘0’-write operation, V_{BL} is pulled down to 0 V , hence V_{th-P2} is lowered by the forward body-bias: $|V_{BS-P2}| = V_{DDM}$. The lowered V_{th-P2} improves the charge current at V_2 , which shortens the access time. On the other hand, V_{th-P1} is raised due to the reverse body-bias: $|V_{BS-P1}| = V_{DD} - V_{DDM}$, where the body voltage of P1 (V_{B-P1}) is higher than the source voltage of P1 (V_{S-P1}) since $V_{B-P1} = V_{DD} > V_{S-P1} = V_{DDM}$. The combination of P1 with higher V_{th} and N1 with normal V_{th} pulls down the curve of INV(L) as shown by the solid curve in Fig. 2 (a), which improves the write margin.

In the read operation based on the LAB scheme, both V_{th-P1} and V_{th-P2} are slightly lowered by the forward body-bias: $|V_{BS-P1}| = |V_{BS-P2}| = V_{DDM} - V_{DD}$ as described in Section 3.1. The combination of pMOS with lower V_{th} and nMOS with normal V_{th} pulls up the curve of INV(L) and shift the curve INV(R) to the right as shown in Fig. 2 (b), which improves the read margin.

4 Simulation results

We have performed SPICE simulations under the conditions that the transistor sizes: $L = 100\text{ nm}$, $W = 160\text{ nm}$, the threshold voltages are set to $V_{th-n} = 0.39\text{ V}$ for nMOS and $V_{th-p} = -0.36\text{ V}$ for pMOS, and the supply voltage is set to $V_{DD} = 0.5\text{ V}$. The capacitances of a word line and a bit line for $256\text{ word} \times 32\text{ bit}$ memory array are determined as $C_{WL} = 11\text{ fF}$

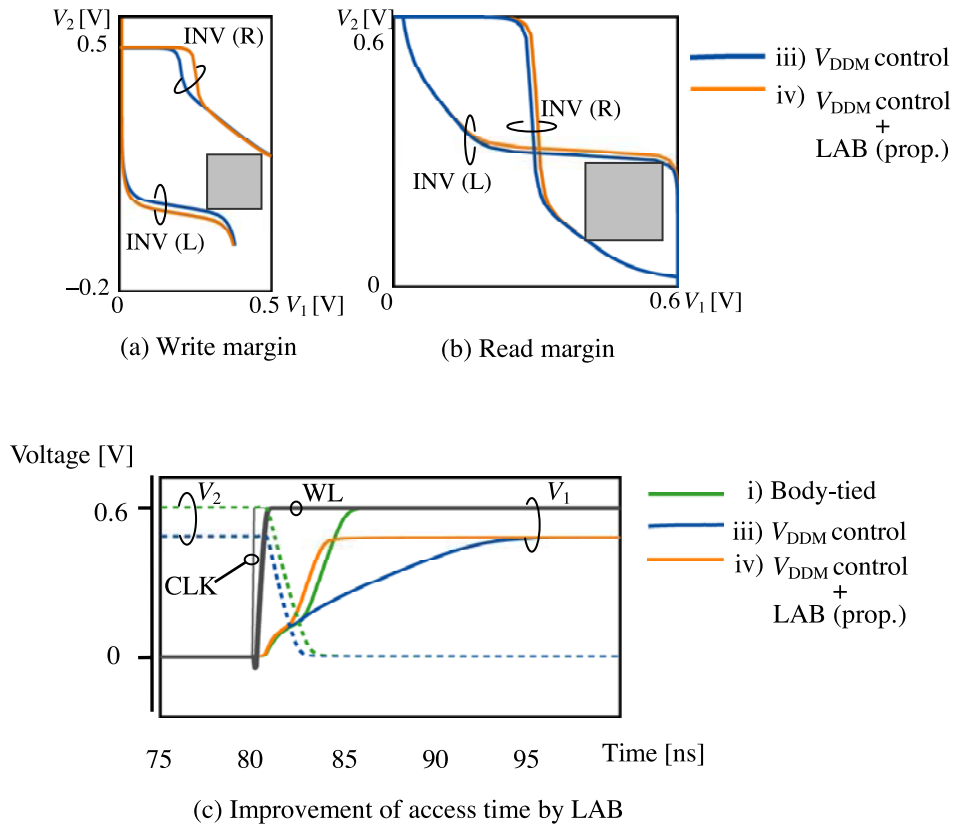


Fig. 2. Impacts of LAB for margins and access time.

and $C_{BL} = 31$ fF, respectively. We have evaluated the access time and the write/read margins by the 1 k-points Monte Carlo simulations for the following four types of SOI-SRAM.

- i) Body-tied without the dynamic V_{DDM} control ($V_{DDM} = V_{DD}$)
- ii) LAB scheme without the dynamic V_{DDM} control ($V_{DDM} = V_{DD}$)
- iii) Body-tied with the dynamic V_{DDM} control
- iv) LAB scheme with the dynamic V_{DDM} control

The dynamic V_{DDM} control with iii) and iv) has been performed by switching the supply voltage to memory cells (V_{DDM}) to $V_{DDH} = V_{DD} + 0.1$ V for read operation, and to $V_{DDL} = V_{DD} - 0.1$ V for write operation, respectively. The standard deviation σ of V_{th} is assumed so that 3σ corresponds to 10% of V_{th} .

Table I shows the results with access time and noise margin. Here, we define the write time as the period from the point of $V_{DD}/2$ in WL during a low to high transition to that in the data retention node of memory cells during the data inverting operation. We also define the read time as the period from the point of $V_{DD}/2$ in WL during a low to high transition to that in the output data signal from Sense Amplifier (BL_{out}).

The body-tied SOI-SRAM with dynamic V_{DDM} control shows 94% longer write time than that without the V_{DDM} control, due to the lowered supply voltage to memory cells during write operation. On the other hand, the proposed SOI-SRAM based on the LAB scheme with the dynamic V_{DDM} control shows 58% shorter write time than the body-tied SOI-SRAM with the dynamic V_{DDM} control.

Table I. Access time and noise margin.

Write / Read	Access time/Margin	w/o V_{DDM} control		w/ V_{DDM} control	
		i) conv.	ii) prop.	iii) conv.	iv) prop.
Write	Write time [ns]	3.12	2.15 (0.69)	6.06 (1.94)	2.55 (0.82)
	Write margin [mV]	92.5	92.5 (1.00)	187 (2.02)	204 (2.21)
Read	Read time [ns]	17.4	17.6 (1.01)	11.6 (0.67)	11.7 (0.67)
	Read margin [mV]	103	103 (1.00)	170 (1.65)	176 (1.71)

i), iii) conv. : Body-tied

ii), iv) prop. : LAB (Look-ahead Active Body-biasing)

() : Ratios to “i) body-tied without the V_{DDM} control”

Table I also shows that the read time with the proposed SOI-SRAM based on iv) the LAB scheme with dynamic V_{DDM} control is 0.1 ns longer than that with iii) the body-tied SOI-SRAM with dynamic V_{DDM} control. This small difference is caused by the slightly increased leakage currents of P1 and P2 due to the lowered V_{th-P1} , V_{th-P2} by the forward biases $|V_{BS-P1}| = |V_{BS-P2}| = V_{DDM} - V_{DD}$.

Fig. 2 (c) shows the waveforms in the write operation with LAB, where the waveform of V_2 (V_{DDM} control + LAB) rises rapidly owing to the increased charge current. Thus, the proposed SOI-SRAM shows 18% shorter write time and 33% shorter read time in comparison with the body-tied SOI-SRAM without the dynamic V_{DDM} control.

In addition, the proposed SOI-SRAM improves the read and write margins by 3.5% and 9.1%, respectively. As described in Section 3.2, the proposed SOI-SRAM cell shifts the curve of INV(L) and INV(R) in Fig. 2 (a), (b), which improves the read and write margins.

5 Conclusion

In this paper, we have proposed a memory cell based on LAB scheme for SOI-SRAM with the dynamic V_{DDM} control. Although conventional V_{DDM} control scheme expands the read and write margins, it suffers from degradation of the access time. The proposed LAB scheme with the dynamic V_{DDM} control uses bitline signals to control V_{th} of appropriate pull-up transistors corresponding to the type of operations: ‘0’-write, ‘1’-write, and read, which shortens the access time while improving the read and write margins.

The simulation results have shown that the write access time is shortened by 58% in comparison with the conventional the dynamic V_{DDM} control.