IEICE Electronics Express, Vol.6, No.9, 546–552

Efficient Carbon Nanotube Galois Field Circuit Design

Peiman Keshavarzian[1a)] **and Keivan Navi**[2b)]

[1] *Ph.D Student, Science & Research Branch, Islamic Azad University, Tehran, Iran.*

[2] *Department of Electrical and Computer Engineering, Shahid Beheshti University, GC, Tehran, Iran.*

a) *Keshavarzian.p@srbiau.ac.ir*

b) *Navi@sbu.ac.ir*

Abstract: For the last couple of decades, multiple-valued logic (MVL) such as ternary logic styles has attracted considerable attention. MVL circuits can reduce the number of operations necessary to implement a particular mathematical function and further have an advantage in terms of reduced area. Carbon nanotube field effect transistors (CNFETs) are being extensively studied as possible successors to Silicon MOSFETs. Implementable CNTFET circuits have operational characteristics to approach the advantage of using MVL in voltage mode. In this paper through using "carbon nanotube field effect transistor" characteristics we present efficient galois field operations. Consequently, the simulation denouements demonstrate the efficient circuit parameters such as chip area, delay, power and power delay product.

Keywords: CNTFET, MVL, nanotube, ternary, galois field, circuit design

Classification: Integrated circuits

References

[1] J. Deng and H.-S. P. Wong, "A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application - Part I: Model of the Intrinsic Channel Region," *IEEE Trans. Electron. Devices*, vol. 54, p. 3186, 2007.

[2] J. S. Hwang et al., "Electronic transport properties of a single-wall carbon nanotube field effect transistor with deoxyribonucleic acid conjugation," *Physica E:Low-dimensional Systems and Nanostructures*, vol. 40, no. 5, p. 1115, March 2008.

[3] P. Keshavarzian and K. Navi, "Universal Ternary Circuit Design Through Carbon Nanotube Technology," *Proc. 2nd International Conference On Nanostructures*, Kish Island, p. 370, March 2008.

[4] A. Raychowdhury and K. Roy, "Carbon-Nanotube-Based Voltage-Mode Multiple-Valued Logic Design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, p. 168, March 2005.

[5] K. Navi, M. H. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two new low power full adders based on majority-not gates," *Microelectronics journal, Elsevier*, vol. 40, p. 126, 2009.

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

[6] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "a novel low power full-adder cell for low voltage," *Integration, the VLSI journal, Elsevier*, to be appeared.

1 Introduction

Nanotechnology is a novel field of research that cuts across many fields – electronics, chemistry, physics and biology that analyzes and synthesizes structures in the nano scale (10^{-9} m) such as nano particles, nanowires, Nanotubes, etc. Nanotubes can be viewed as a rolled-up sheet of graphite. Carbon Nano Tube (CNT) has attracted attention in recent years not only for its relatively small dimensions and unique morphologies, but also for its potential of implementation in many emerging technologies. CNT is one of the several cutting-edge emerging technologies within nanotechnology with high efficiency and a wide range of applications in many different streams of science and technology. Nano-circuits based on CNTs such as CNT Field Effect Transistors (CNTFETs) show big promise of consuming less power and to be much faster than available silicon based FETs. The outline of this paper is as follows. In section 2, MVL outlines are described, in section 3 CNT field effect transistors (CNTFET) are inspected, in section 4 efficient Galois field design, its implementation and its simulation results are presented. Conclusions are demonstrated in section 5.

2 Multiple Valued Logic

MVL has been intensively used in computer arithmetic literature [5, 6]. Binary Galois field circuits have been investigated by many researchers. Much less work has been done on MVL versions of such circuits. The first implementation of multiple valued Galois field operations is reported by Dao in 1984. A *field* (F, +, *) is a set with two operations that are closed with respect to that set. We will call them addition and multiplication. A certain number of axioms, ensuring the existence of neutral (zero for the addition operation and one for multiplication) and inverse elements with respect to both operations, as well as commutativity and distributivity of multiplication with respect to addition, define the structure of the field. The operations "+" and "*" together with the set F are said to form *groups* (F, +) and (F- {0}, *), where the group is defined as a set with the operation that is closed with respect to that set. The axioms of a group guarantee that there is a unique neutral element, as well as the inverse element for each member of the group. All fields such as *Galois fields* contain a finite number of elements. In the case of a field with a prime number of elements, both operations are defined as usual modulo addition and multiplication.

Furthermore let us consider an r-valued n-variable function f(X), where $X = \{x_1, x_2, \ldots, x_n\}$ and each x_i can take up values from $R = \{0, 1, \ldots, r-1\}$. Thus the function f(X) is a mapping $f : R^n \rightarrow R$. There are r^{r^n} different

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

functions possible in the set f. A set of primitive functions is explained as the Literal set [4]: A MIN (minimum) operator, a TSUM (truncated sum) operator, a complement, a cycle (or a clockwise cycle) and a literal of a multivalued variable, as shown below:

$$ {}^{a}(X)^{b} = \begin{cases} high & a < X < b \\ low & otherwise \end{cases}, \; TSUM(a1,\, a2) \;=\; \min(a1 + a2\,,\, r - 1) \tag{1} $$

3 Carbon-nanotube Field-Effect Transistor

The first carbon-nanotube, field-effect transistor (CNTFET) was reported in 1998. At that time, it was not clear how these devices worked, but subsequent progress has been rapid. Today, sophisticated transistor structures demonstrating the potential for high performance are appearing, and sophisticated modeling techniques are being used to understand their physics. A CNT was positioned so as to bridge two gold or platinum electrodes, which acted as the source and drain of the FET. Carbon nanotube field effect transistors (CNTFET) present large potential as building blocks for specific applications in the area of nanoelectronics, carbon nano-electronics [2] may be faster than conventional Si, SiGe, GaAs, or InP semiconductor technologies that are predicted to have a cut off frequency of 80 GHz/L, where L is the gate length in microns, opening up the possibility of a ballistic THz nanotube transistor. Field effect transistor devices with carbon nanotube conducting channels have been developed and used for biosensing and biodetection and exhibited strong memory effects.

The contact between metal and CNT can be of Ohmic or Schottky type, the CNT used in the transistor was a semiconducting SWNT that can be switched from metallic to insulating state by modulation of the gate voltage. There are two types of carbon-nanotube transistors that are being extensively studied. One of them is a tunneling device that works on the principle of direct tunneling through a Schottky barrier at the source–channel junction. The barrier width is modulated by application of the gate voltage, thus transconductance of the device is dependent on the gate voltage. Two important characteristics of these nanotube transistors are worth mentioning: energy barrier and Schottky-barrier. CNTFETs exhibit strong ambipolar characteristics, and this constrains the use of these transistors in conventional CMOS logic families. To overcome these disadvantages associated with Schottky barrier CNTFETs, there have been attempts to develop CNTFETs which would behave like normal MOSFETs. These attempts have met significant success so far and the promise is enormous, the MOSFET-like CNTFET operates on the principle of barrier height modulation by application of the gate potential.

More recently, Guo *et al.* have presented numerical studies on such MOSFET-like CNTFETs, and it is evident that: unlike Schottky-barrier field-effect transistors (FETs) the MOSFET-like CNTFETs have unipolar characteristics; absence of the Schottky barrier reduces OFF leakage current;

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

they have more scalability compared to their Schottky-barrier counterparts and in the ON state the source-to-channel junction has no Schottky barrier and thus a significantly higher ON current. Further, it can be assumed that transportation through these CNTFETs is ballistic. In this paper, we will consider the non-Schottky-barrier MOSFET-like unipolar CNTFET with ballistic transport as our device of interest. Henceforth, in this paper, the abbreviation CNTFET will be used to mean such a MOSFET-like device unless otherwise is mentioned.

This geometry-dependent threshold voltage has been exploited in this study to obtain CNTFETs that turn on at different voltages depending on their diameters. Therefore, in this paper, we have used a dual-diameter CNTFET-based design for the ternary logic implementation.

4 Efficient Galois Field Circuit Design

Since many multiple-valued circuits over ternary Galois field or Literal set can be synthesized using addition and multiplication operations in the galois field and literal set operations that were described before, thus these basic operators can be used in multiple-valued implementations whenever they are applied. In simpler word, the MVL functions should be demonstrated by a combination of the basic operators in the galois field or literal set [3]. For example the galois field adder and multiplier in the literal set should be demonstrated by using the appropriate combination of the basic operators in the literal set as follow:

$$\begin{aligned} '+' \approx Tsum(&Tsum(Tsum(\min[^0(A)^0, ^1(B)^1], \min[2^0(A)^0, ^2(B)^2]),\\ &Tsum(\min[^1(A)^1, ^0(B)^0], \min[2^1(A)^1, ^1(B)^1])\ ),\\ &Tsum(\min[2^2(A)^2, ^0(B)^0], \min[^2(A)^2, ^2(B)^2])). \end{aligned} \tag{2}$$

$$\begin{aligned} '*' \approx Tsum(&Tsum(\min[^2(A)^2, ^2(B)^2], \min[2^2(A)^2, ^1(B)^1]),\\ &Tsum(\min[^1(A)^1, ^1(B)^1], \min[2^1(A)^1, ^2(B)^2])). \end{aligned} \tag{3}$$

As an example attaining these two functions (Eq. (2), (3)) in the literal set consume 96 transistors with 60 resistors for Adder and 68 transistors with 44 resistors for Multiplier. In comparison with the literal set design we have achieved efficient galois field adder and multiplier.

In this design for the ternary logic implementation we employ 12 transistors (8 transistors + 4 transistors for input complementary) with 6 resistors (2 resistors + 4 resistors for input complementary) for Galois field Multiplier and 16 transistors (12 transistors + 4 transistors for input complementary) with 6 resistors (2 resistors + 4 resistors for input complementary) for Galois field Adder to approach the efficient galois field adder and multiplier.

In this design, we use CNTFET transistors with resistive pull-ups. Our nanotube transistors have two different diameters with two different threshold voltages, consequently. According to input voltage level, and two different threshold voltages as $V_{th1} = 0.25^V$ and $V_{th2} = 0.58^V$, we will have three different states. If $V_{input} < V_{th1} = 0.25^V$, both transistors will be turned off. If input voltage rises to $V_{th1} = 0.25^V < V_{input} < V_{th2} = 0.58^V$, just one

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

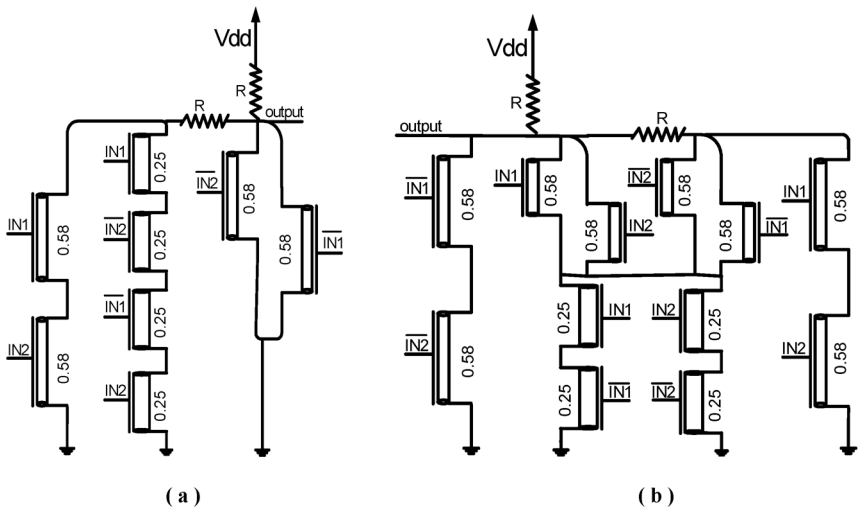

Fig. 1. Efficient Galois field circuit design. a) Galois field Multiplier. b) Galois field Adder. (CNTFETs contains its Threshold voltage)

of the transistors will be turned on. If input voltage rises further more to $V_{input} > V_{th2} = 0.58^{V}$, both transistors will be turned on. Hence analyzing our new design shows that, output voltages are result of voltage divisions which are produced by combination of these resistors and active transistors.

For each combination of inputs only one predominant output path is activated. Therefore through our circuit design structure appropriate voltage division held the output at the expected stable voltage.

In this paper, a compact model of CNTFETs has been used and simulations have been carried out using HSPICE. The details of the modeling technique are available in [1]. Short channel MOSFET like CNTFETs are of particular interest because they are shown to provide near ballistic current, thereby indicating maximum performance. The carrier density for any sub-band of such nanotube transistor can be expressed as,

$$n_p = \int_{E_{c,p}}^{\infty} \frac{D_{p(E)}}{2} [\, f(E-\mu_S) + f(E-\mu_d)]dE \tag{4}$$

Where $\mu_{s(d)}$ is the source (drain) Fermi level, Ec, p be the conduction band minimum for the p_{th} sub-band, $f(E)$ is the probability that a state with energy E is occupied and $D(E)$ is the nanotube density-of-states. Though solving Eq. (4) analytically is not possible, an approximate closed form solution can be obtained by dividing the operating condition into two parts. For $\psi_s < \psi_T$ (below threshold), when $\sqrt{z^2+\varepsilon_{c,p}^2} - \varphi_z \gg 1$ for all $'z' : 0 \to \infty$ Eq. (4) can be approximated to calculate the charge as

$$Q_{CNT} = qN_0 \left[\sum_P \int_0^{\infty} e^{-(\sqrt{z^2+\varepsilon_{C,P}^2})} dz\right] (1+e^{-v_{ds}})\, e^{\varphi_s} = e^{\alpha_0+\varphi_s} \tag{5}$$

The integral of Eq. (5) can be precomputed numerically and α_0 can be analytically obtained for any drain voltage. For $\psi_T < \psi_s \leq E_{C,P}/q$ (above

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

threshold), we can obtain Q_{CNT} as,

$$\begin{aligned} Q_{CNT} &= qN_0 \sum_P \sum_{n=1}^{\infty} \left[(-1)^{n-1} e^{n(\varphi s - \varphi T)} (1 + e^{-nvds}) \int_0^{\infty} e^{-n(x-\varphi T)} dz \right] \\ &\approx \lambda_0 + \eta_1 \lambda_1 (\psi_s - \psi_T) + \eta_2 \lambda_2 (\psi_s - \psi_T)^2 \end{aligned} \tag{6}$$

the drain current, I_{ds} and gate input capacitance, C_G can be easily obtained as follows.

$$\begin{aligned} I_{ds} &= \frac{4qk_BT}{h} \sum_p [\ln(1 + e^{-\xi s}) - \ln(1 + e^{-\xi d})] \\ and \;\; C_G &= \frac{\partial Q_{CNT}}{\partial V_{gs}} \\ where \; \xi_i &= \frac{q\psi_s - E_{c,p} - qV_i}{k_bT} (i = s, d) \end{aligned} \tag{7}$$

The parasitic capacitance in CNTFETs, consists of mainly the gate/source and gate/drain fringe capacitances. The other components such as gate to substrate and source/drain to substrate capacitances are expected to be very small and hence, are neglected in the analyses. The fringe capacitance (Cfr) of this geometry can be analytically calculated using the following equation.

$$\begin{aligned} C_{fr} &= \frac{2\varepsilon W}{\pi} \ln \left[\frac{T_{g,s/d} + \eta T_g + \sqrt{L_{un}^2 + (\eta T_g)2 + 2T_{g,s/d}\,\eta T_g}}{L_{un} + T_{g,s/d}} \right] \\ &+ \frac{k\varepsilon W}{\pi} \ln \frac{\pi W}{\sqrt{L_{un}^2 + T_{g,s/d}^2}} e^{\left| \frac{L_{un} - T_{g,s/d}}{L_{un} + T_{g,s/d}} \right|} \\ where \;\; \eta &= \exp \left[(L_{sd} + L_{un} - \sqrt{L_{un}^2 + T_g^2 + 2t_{g,s/d}\,T_g})/\tau\, L_{sd} \right] \end{aligned} \tag{8}$$

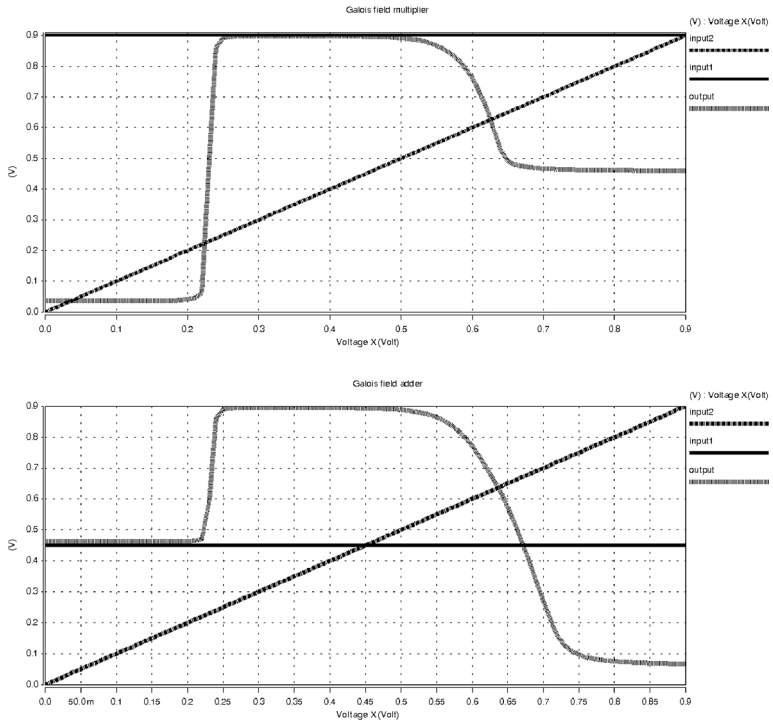

Fig. 2. A sample of Galois field (multiplier / adder) simulation result

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009

Simulation results show reduction in terms of power consumption, chip area, delay and improvement in speed by using galois field as the new MVL field circuit design. We compare simulation results with the state-of-the-art circuit design in the literal set. The comparison results are listed in table I.

Table I. comparison results [a] literal set [4] [b] new galois field circuit design

	Average Delay (PS)	Average Power (μW)	PDP (J)
Galois field adder [a]	287.231	103.800	2.981 e-14
New Galois field adder [b]	51.172	11.290	5.777 e-16
Galois field multiplier [a]	232.420	77.740	1.806 e-14
New Galois field multiplier [b]	41.77	12.590	5.258 e-16

5 Conclusion

In this paper we have presented our new Galois field circuit design using carbon nanotube field effect transistors. We have achieved a significant improvement in the number of circuit elements as well as chip area, power and speed. Also this design exhibit the efficient field area, through galois filed adder and multiplier in the multiple valued-logic using carbon nanotube field effect transistors.

DOI: 10.1587/elex.6.546
Received February 28, 2009
Accepted March 31, 2009
Published May 10, 2009