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An energy efficient full adder cell for low voltage

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Abstract: This paper presents an area efficient, high-speed and ultra low power 1-bit full adder that uses only 9 transistors. It works based on majority function and MOS capacitors. Because of the simple structure of the proposed design and reduced transistor counts, a very low power full adder is realized. It also can work more reliably at ultra low supply voltage in comparison with the previous designs. The circuit being studied is optimized for energy efficiency at 0.18-μm CMOS process technology. The adder cell is compared to four standard adders based on power consumption, speed and power delay product. Intensive simulation runs on HSPICE shows that the new adder has more than 44% in power savings over conventional CMOS adder and is 10% faster.

Keywords: full adder, low power, very large-scale integrated (VLSI) circuit, majority function and performance analysis

Classification: Integrated circuits

References

[1] C. H. Chang, J. Gu, and M. Zhang, "A review of 0.18um full adder performances for tree structure arithmetic circuits," *IEEE Trans. VLSI Syst.*, vol. 13, no. 6, June 2005.

[2] K. Navi, M. h. Moaiyeri, R. F. Mirzaee, O. Hashemipour, and B. M. Nezhad, "Two New Low-Power Full Adders Based on Majority-not Gates," *Microelectronics Journal*, Elsevier, vol. 40, no. 1, pp. 126–130, Jan. 2009.

[3] K. Navi, R. F. Mirzaee, M. H. Moaiyeri, B. M. Nezhad, O. Hashemipour, and K. Shams, "Ultra high speed Full Adders," *IEICE Electron. Exp.*, vol. 5, no. 18, pp. 744–749, 2008.

[4] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, "A novel low power full-adder cell for low voltage," To be appeared in Elsevier, *Integration, the VLSI Journal.*

[5] J. T. Kao and A. P. Chandrakasan, "Dual-threshold voltage techniques for low-power digital circuits," *IEEE JSSC*, 35(7): pp. 1009–1018, July 2000.

[6] H. Aminzadeh, R. Lotfi, and K. Mafinezhad, "Low-cost area-efficient low-dropout regulators using MOSFET capacitors," *IEICE Electron. Exp.*, vol. 5, no. 16, pp. 610–616, 2008.

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1 Introduction

Today, there are an increasing number of portable applications with limited amount of power available, requiring small-area low-power high throughput circuitry. Therefore, circuits with low-power consumption become the major candidates for design of microprocessors and system-components. The research effort in low-power microelectronics has been intensified and low-power VLSI systems have emerged as highly in demand.

Addition is one of the fundamental arithmetic operations and it is used extensively in many VLSI systems [1, 2, 3, 4]. In additions to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation. In most of these systems the adder is part of the critical path that determines the overall performance of the system. So building low-power, high-performance adder cells is of great interest.

Lowering the supply voltage appears to be the most eminent means to reduce power consumption. However, lowering supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption.

The goal of this work is to design an area efficient circuit based on 0.18-μm CMOS process technology that can operate at ultra low power supply voltage and to avoid any degradation on the output voltage, have less delay in critical path, and be noise immune even at low supply voltage. One of the most important obstacles in decreasing supply voltage is the large transistor count but this new full adder, uses only 9 transistors.

The rest of this paper is organized as follows: in Section II we review some existent implementations of the full-adder cell. Then in Section III, we present the 1-bit full-adder cell. In Section IV, the circuits are simulated and the simulation results are analyzed and compared. Finally, Section V concludes the paper.

2 Some previous full adders

Different logic styles for implementing full adder cell tend to favor one performance aspect at the expense of the other. Although all logic styles do the identical function, but the method of generating the middle nodes and the transistor count are varied. Results are compared with the following designs including previous works and some conventional full adder cells.

The complementary CMOS full adder (C-CMOS) [1] as shown in Fig. 1 (a) generates *Cout* throughout a single static CMOS gate. It is based on conventional pull-up and pull-down transistors. The series transistors in the output stage form a weak driver. Therefore, additional buffers at the last stage are required to provide the necessary driving power to the cascaded cells. The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing.

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10T in Fig. 1 (b) [1] generates and uses A_{XOR} B and invert of it as a select signal to produce the outputs. It benefits from small transistor count but it must be notified that this full adder is based on pass transistor logic style and suffers from double V_T loss problem and cannot work properly when supply voltage is less than 1.8 V.

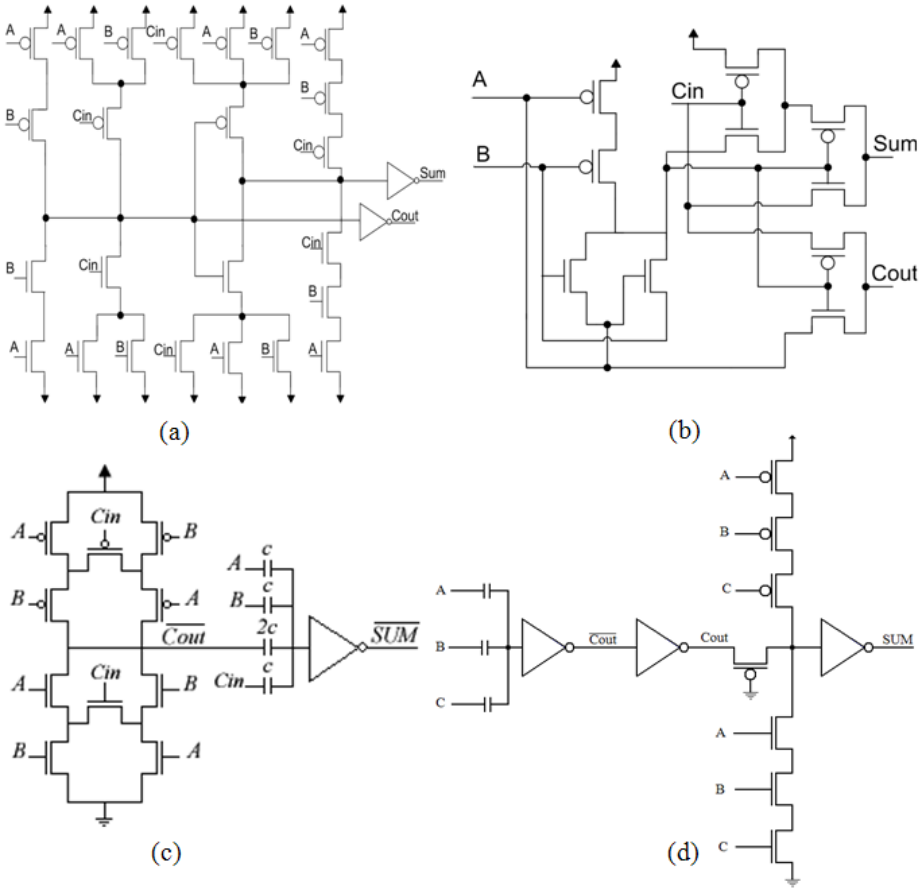

Fig. 1. (a) Conventional CMOS Adder. (b) 10T Adder. (c) Bridge Style-Based Adder. (d) 13T Adder.

Fig. 1 (c) and Fig. 2 (d) illustrate Bridge Style-Based (BSB) adder [2] and 13T adder [3] respectively. These designs eliminate the time consuming XOR and XNOR gates. The basic idea of Bridge Style-Based adder is that the *Cout* can be implemented by a 3-input Majority Function and also *SUM* can be generated by $\overline{Cout}$ using a 5-inputs Majority Function with *A*, *B*, *C* and two $\overline{Cout}$ inputs. In this design, the first majority-not gate is implemented with a high performance CMOS bridge circuit. The main idea of 13T full adder cell is based on the similarity between the min-terms of *Cout* and $\overline{SUM}$ functions. They only differ in $A.B.Cin$ and $\overline{A}.\overline{B}.\overline{Cin}$ min-terms. The three series transistors at the output stage in the pull-up and pull-down networks correct the *Cout* function to create $\overline{SUM}$ output. Both of these adder cells benefit from low power dissipation due to their transistor counts but they suffer from lack drivability, and so by cascading such circuits the performance will degrade. Additional buffers at the last stage of 13T are needful to provide

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the required driving power because of having six transistors from Vdd to the ground in the output stage similar to C-CMOS that reduce driving capability and speed of the circuit. Since the outputs of Bridge Style-Based adder are $\overline{Cout}$ and $\overline{SUM}$, two Inverters are attached to make it comparable with the other cells. Extra inverters increase the short-circuit power as well as delay and power consumption but they also enhance the driving capability of the adder cell in our test-bench.

3 The proposed full adder design

The full adder operation can be stated as follow: given the three input A, B and C, it is desired to calculate two 1-bit outputs, SUM and $Cout$. $Cout$ can be implemented with a three-input Majority Function. This fact is also proposed in Eq. (1).

$$Cout = AB + AC + BC \tag{1}$$

SUM is different with Majority Not Function in only two places; when inputs are 000 or 111. Therefore SUM can be calculated with $\overline{Cout}$ as shown in Eq. (2).

$$SUM = A \oplus B \oplus Cin = \overline{Maj}(A, B, Cin).(A + B + Cin) + A.B.Cin = \overline{Cout}(A + B + Cin) + ABCin \tag{2}$$

Fig. 2 (a) illustrates the proposed adder cell. It is based on low power design of majority not function with classical CMOS inverter and capacitors. $Cout$ has been implemented by means of three input capacitance plus an inverter gate as a Majority Not Function. The pull-up and pull-down networks in previous design, Fig. 1 (d) consist of three series transistors have substituted by a high-Vt transistor [3, 5]. The threshold voltage of this kind of transistor is more than the conventional ones. Therefore the NMOS transistor as pull down network is turned on ($Vgs_n > Vth_n$) and the output is become low only when the three inputs are high and vice versa while all of the inputs are low the PMOS is on ($Vgs_p < Vth_p$). In all states except $A.B.Cin$ and $\overline{A}.\overline{B}.\overline{Cin}$ both pull-up and pull-down transistors are switched off and the majority path creates the Sum output. The switched-on PMOS pass-transistor operates as a resistance [3]. It corrects the voltage difference in the two exceptional min-terms. The last CMOS inverter enhances the final voltage levels and creates the SUM function. By using this method the number of transistors has been reduced to 9 so, the proposed circuit has less area comparing to other designs. It has low transistor count results in low switch capacitance reduction and the capability of working at ultra low supply voltage. Operating properly at this range of supply voltage without V_T loss problem, having only two transistors from Vdd to the ground instead of six transistors and taking advantage from using three robust CMOS inverter make it a good choice for implementing low power design. As shown in Fig. 2 (a) each of the adder inputs are connected to only one capacitor which results in improving the reliability of the whole circuit and there is not any fan-out problem for the drivers of the adder [4]. The new design is

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robust against supply voltage variation. The circuit also is a ratio less one moreover, the energy consumed per switching activity is better. It benefits from good drivability so it can be cascaded easily whereas the performance of the previous designs in Fig. 1 degrade when they are cascaded.

To design the proposed circuit layout which consists of three input capacitors, various techniques for constructing capacitors have been investigated. This proposed circuit's capacitors have been implemented using the MOS capacitors (MOSCAP) available in the 0.18 μm CMOS process technology [6]. Tying the drain and source of a MOSFET together makes a MOSCAP. The length of the gate of the MOSCAP determines the capacitance value. The overlap, sidewall and fringe capacitances are between the gate and the drain or source. These capacitances are only dependent on the width of the MOSCAP. Gate to channel capacitance is dependent upon the area of the channel, or the MOSCAPs width and length. So the capacitance of the MOSCAP is directly dependent on the length. A linear increasing of the capacitance occurred by increasing the length of the MOSCAP in a linear manner. Simulations show that most suitable value for the capacitors in the structure of proposed circuit is around 9 fF [3]. Fig. 2 (b) exhibits

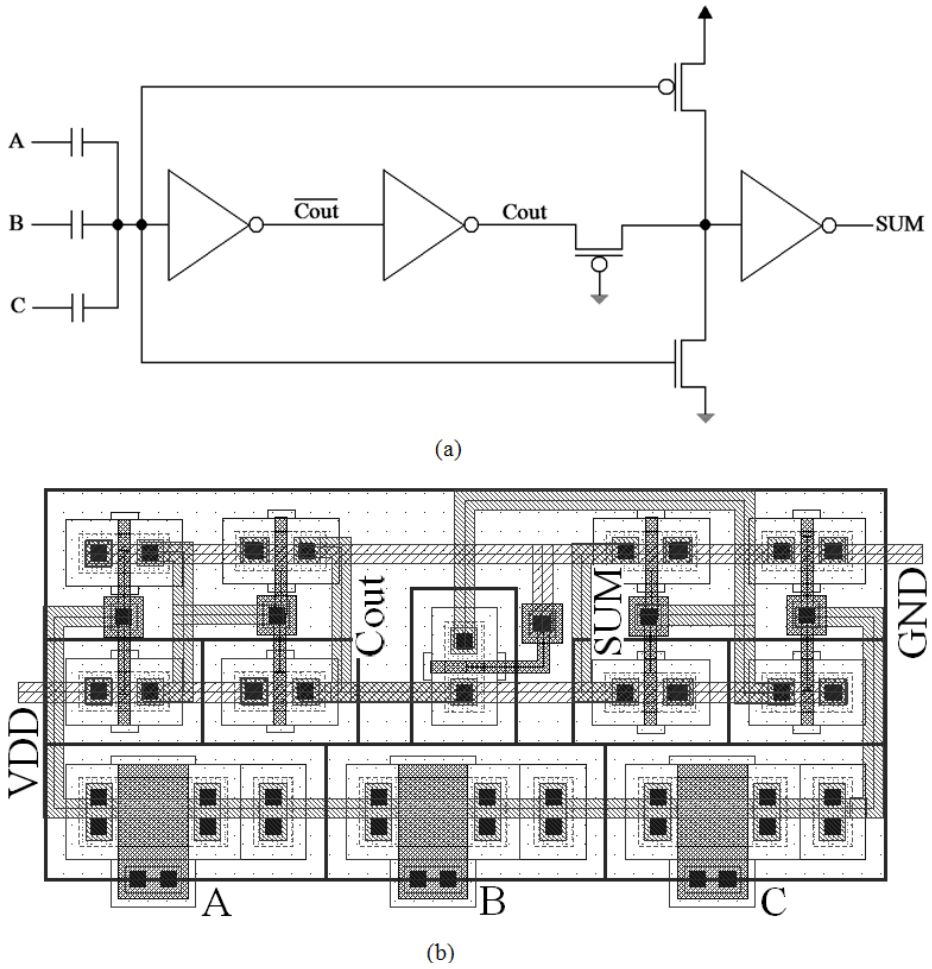

Fig. 2. (a) The proposed full adder cell. (b) Compact layout of the new full adder.

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the compact layout of the presented adder cell. As shown in this figure the presented full adder uses only two metal lines.

4 Simulation results

Five 1-bit full adder cells including C-CMOS, 10T, Bridge Style-Based, 13T and the proposed adder, have been simulated using HSPICE with 0.18 μm CMOS technology. The test-bench is different with [3] and it has been made of five cascaded adder cells. This structure simulates the circuits like regular multipliers and binary adders that use full adder cells as the building block. The inputs are fed from the buffers (two cascaded inverters) to give more realistic input signals and the outputs are loaded with buffers to give proper loading condition. The performance of the full adder circuits in terms of worst-case delay, power consumption and power delay product under different supply voltages (0.8 V, 1.3 V and 1.8 V) at 100 MHz frequency is evaluated and presented in Table I. The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output for both rise and fall output transitions. For the calculation of the power-delay product, worst-case delay is chosen to be the larger delay amongst the two outputs. This is done over all the 64 possible transitions for an accurate result. More ever these 64 input patterns applied to the cells, for measuring the average power consumption of the cells. Buffers are attached to the 10T and 13T to enhance their driving capability. By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of all adders without significantly increasing the power consumption, and transistor sizes can be set to achieve minimum PDP.

Table I shows that the proposed design has the best PDP and power consumption in comparison with others. It consumes 44%, 40% and 35% less power than the C-CMOS at 0.8 V, 1.3 V and 1.8 V supply voltages respectively. This design also has the minimum delay at 0.8 V and it exhibits that the proposed adder is the most suitable design for working at low supply voltages toward other designs.

Table I. Simulation results.

	0.8V			1.3V			1.8V		
	Power (µW)	Delay (nS)	PDP (fJ)	Power (µW)	Delay (nS)	PDP (fJ)	Power (µW)	Delay (nS)	PDP (fJ)
C-CMOS	0.887	0.673	0.597	2.848	0.307	0.8743	6.287	0.157	0.9871
10T	-	-	-	-	-	-	8.731	0.162	1.4144
BSB	0.592	0.645	0.3818	1.82	0.349	0.6352	4.263	0.183	0.7801
13T	0.637	0.658	0.4123	2.044	0.351	0.7174	4.32	0.197	0.851
Proposed	0.493	0.603	0.2973	1.711	0.321	0.5492	4.065	0.158	0.6423

5 Conclusion

In this paper the previous works has been improved to make a high speed and ultra low power adder cell which can operate perfectly at very low range of power supply voltage. This adder takes advantage of using just four robust

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CMOS inverter and it has only two transistors from *Vdd* to the ground so the critical circuit paths is reduced.

HSPICE Simulations have been performed by using a 0.18 μm technology under a cascaded test-bench to evaluate the new design. Results show the presented adder has the best PDP in comparison with the others. This adder consumes 44%, 40% and 35% less power compared to C-CMOS at low power supply. Consequently, this new design is appropriate to be applied for construction of large low power high performance VLSI systems.

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