IEICE Electronics Express, Vol.6, No.11, 736–742

CMOS cross-coupled charge pump with improved latch-up immunity

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Abstract: In this paper, a novel CMOS charge pump with substantially improved immunity to latch-up is presented. By utilizing a dedicated bulk pumping and blocking (DBPB) technique, the proposed charge pump achieves greatly reduced forward voltage of source/drain-substrate junction of transistors, resulting in decreased charge loss and increased latch-up immunity. Comparison results indicated that the maximum bulk forward voltage of the proposed charge pump was less than 0.05 V (88% improvement) for zero output current during power-up, and less than 0.12 V (88% improvement) regardless of the amount of output current during ordinary pumping operation.

Keywords: bulk forward, charge pump, latch-up, voltage doubler

Classification: Integrated circuits

References

[1] J. F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, pp. 374–378, June 1976.

[2] T. B. Cho and P. R. Gray, "A 10-bit, 20 Msample/s, 35 mW pipeline A/D converter" *IEEE J. Solid-State Circuits*, pp. 166–172, March 1995.

[3] R. C. Fang and J. L. Moll, "Latch-up model for the parasitic p-n-p-n path in bulk CMOS," *IEEE Trans. Electron Devices*, vol. ED–31, pp. 113–120, Jan. 1984.

[4] P. Favrat, P. Deval, and M. J. Declercq, "A high efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, pp. 410–416, March 1998.

[5] S. Cho, J. Lee, H. Park, G. Lim, and Y. Kim, "Two-Phase Boosted Voltage Generator for Low-Voltage DRAMs," *IEEE J. Solid-State Circuits*, pp. 1726–1729, Oct. 2003.

[6] M. Hsieh, Z. Wang, H. Lin, and Y. Lin, "A new dual pumping circuit without body effects for low supply voltage," *Proc. IEEE Int. Symp. Circuits Syst.*, 2004, vol. ED–2, pp. II–621–4, May 2004.

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
Published June 10, 2009

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1 Introduction

CMOS charge pumps generating dc voltages higher than the supply voltage have been widely used in integrated systems like DRAM, EEPROM, and flash memory. In these charge pumps, nMOS transistors have been usually used as transfer switches to transfer the voltage higher than the supply voltage to the output [1]. Important reasons for using nMOS transistors as transfer switches are to provide with higher carrier speed and to eliminate the influence of parasitic devices by automatic reverse bias of the source-substrate junction. However, insufferable drawback of using an nMOS transistor is the pumping gain degradation due to body effect-induced threshold voltage drop. One method to overcome this problem is to use a pMOS transistor as a transfer switch [2]. In this case, the bulk bias of the pMOS transfer switch must be kept equal to or higher than its source and drain voltages. If once the p-n junction of the transistor becomes forward-biased due to too low bulk potential, the current flowing into substrate raises local substrate potential, sharply increasing the possibility of latch-up [3].

For preventing latch-up in charge pumps due to bulk forward bias, several techniques have been proposed. The conventional CMOS cross-coupled charge pump proposed by Pierre Favrat [4] uses a bulk commute switch to ensure the reverse bias of the junction. After several cycles from the start-up of the charge pump, the pMOS bulk bias is set to a higher voltage between source and drain of the transistor. However, before a sufficiently high voltage at the bulk is reached during power-up transient, the conduction of p-n junction can cause the substrate current, resulting in a charge loss from the boosted node. This substrate current may then eventually cause a latch-up which may burn out the chip. Moreover, even after the output of the charge pump has reached to the target voltage, the pMOS bulk potential can fluctuate severely if the output load draws too large amount of current from the charge pump. This bulk potential fluctuation may also cause the bulk forward problem in the charge pump, increasing the possibility of latch-up. The two-phase boosted voltage generator [5] employs a bulk-potential bootstrapping circuit (BPBC) to make the p-n junction always reverse-biased during the steady state. However, this scheme still causes the bulk forward problem during power-up since the voltages of the pMOS bulk and output nodes are lower than that of the boosting node for the very first several cycles just after starting the power-up sequence. The dual-branch pumping circuit [6] with high voltage clocks (HVC) adopts a bulk precharging circuit before the charge pump starts to operate. However, this circuit cannot bias the pMOS bulk sufficiently high because the bulk precharging level is less than $2V_{DD}$ (actually $2V_{DD} - V_{TH}$). One-time boosting for bulk precharging is also not enough to force the bulk to have a sufficiently high voltage level to prevent latch-up. The circuit also has a problem that, at the very first cycles during power-up, the voltage of the bulk is directly pulled down due to the reverse current to the boosting node.

To avoid the pMOS bulk forward problem during the entire period of

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
Published June 10, 2009

charge pump operation, a novel CMOS cross-coupled charge pump utilizing a dedicated bulk pumping and blocking (DBPB) technique is proposed. In Section 2, we review parasitic devices of the pMOS transfer switch in the conventional CMOS charge pump, and describe issues related to charge loss and latch-up. In Section 3, the proposed CMOS charge pump to reinforce latch-up immunity is described. Simulation results and comparisons are presented in Section 4. Finally, conclusions are given in Section 5.

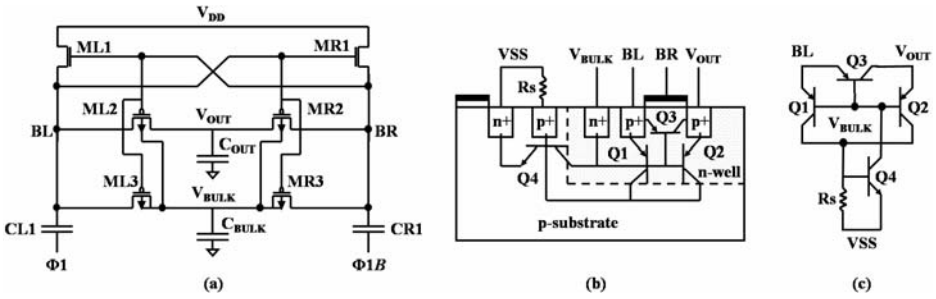

Fig. 1. (a) Conventional CMOS cross-coupled charge pump [4], (b) cross-sectional view of the pMOS transfer switch (ML2), and (c) its equivalent circuit.

2 Parasitic devices in conventional CMOS charge pump

Figure 1 (a) shows the conventional CMOS cross-coupled charge pump reported in [4]. Boosting nodes, BL and BR, are capacitively coupled to clock pulses, $\Phi 1$ and $\Phi 1B$, through pumping capacitors, CL1 and CR1, respectively. Output and bulk nodes, V_{OUT} and V_{BULK}, respectively having reservoir capacitors, C_{OUT} and C_{BULK}, for restraining voltage fluctuations, are boosted by charge-sharing with the associated boosting nodes through transfer switches, ML2, MR2, ML3 and MR3. The cross-sectional view of one of the pMOS transfer switches (ML2) is shown in Fig. 1 (b), and its equivalent circuit is shown in Fig. 1 (c). The equivalent circuit consists of three parasitic p-n-p bipolar transistors, Q1–Q3, one parasitic n-p-n bipolar transistor, Q4, and a parasitic resistor, Rs [4]. Resistor Rs models the parasitic resistance of the local p+ guard ring and the substrate. In the case that p+ guard ring becomes too narrow by process scaling, Rs will become high. The emitter of Q4 biased to GND corresponds to the n+ diffusion in nMOS transistors of nearby circuits or in the nMOS capacitors of the charge pump. Note that, in this charge pump, the transient response of the bulk node is somewhat delayed in comparison to that of the associated boosting nodes since they are connected to each other through the transfer switches having non-zero on-resistance. Due to this delayed transient response of the bulk node, the source-bulk junction of ML2 could become forward biased especially in the first several cycles during power-up since in this period V_{BULK} stays usually at a zero potential. This means that the emitter-base junctions of Q1 and Q2 in the equivalent circuit shown in Fig. 1 (b) become forward biased, and

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
Published June 10, 2009

the surging current to the collector common to these transistors is injected into Rs. Then, as the voltage drop across this parasitic resistor becomes large enough to make Q4 on, a low impedance p-n-p-n path is established, resulting in a latch-up condition [3]. Even if Q4 is not sufficiently turned on, the p-substrate current contributes to pumping charge loss, decreasing the ramp-up speed.

3 Proposed CMOS cross-coupled charge pump

Figure 2 (a) shows the structure of the proposed CMOS cross-coupled charge pump to improve latch-up immunity. Bulk blocking switches, ML4 and MR4, gated by local control signal BSC are used in series with charge transfer switches, ML3 and MR3, respectively, to separate the pMOS bulk from the boosting nodes. Fig. 2 (b) shows a dedicated bulk booster for boosting V_{BULK} and BSC, which consists of an asymmetric cross-coupled charge pump using only nMOS transistors free of bulk forward problem and a blocking control circuit (BCC). The control clock generator for the proposed charge pump is shown in Fig. 2 (c), in which a set of local clocks such as $\Phi 1/\Phi 1B$, $\Phi 1_{AUX}/\Phi 1B_{AUX}$, and $\Phi 1D_{AUX}$ are generated.

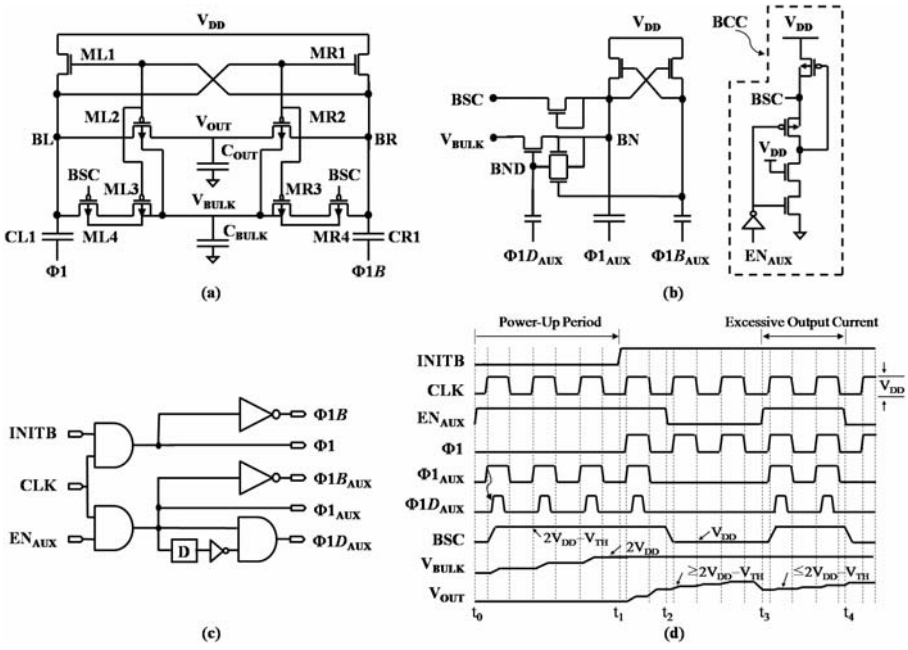

Fig. 2. The structure of the proposed CMOS cross-coupled charge pump: (a) main charge pump, (b) bulk booster, (c) control clock generator, and (d) timing diagram.

Let us explain the operation of the proposed charge pump using the timing diagram shown in Fig. 2 (d). INITB stays low during the power-up period (from t_0 to t_1), disabling main control clocks $\Phi 1$ and $\Phi 1B$ to deactivate the main charge pump. During this period, EN_{AUX}, which becomes high when V_{OUT} is less than $2V_{DD} - V_{TH}$, enables auxiliary clocks $\Phi 1_{AUX}$, $\Phi 1B_{AUX}$,

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
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and $\Phi 1D_{AUX}$ (a pulsed version of $\Phi 1_{AUX}$) to activate the bulk booster. Then, boosting node, BN, of the bulk booster is boosted to $2V_{DD}$, allowing both BSC and BND to be pulled up to $2V_{DD} - V_{TH}$. The pull-up of BSC makes blocking switches ML4 and MR4 turned off, separating V_{BULK} from BL and BR. Every time when $\Phi 1D_{AUX}$ goes up, BND is pulled up toward $3V_{DD} - V_{TH}$, allowing V_{BULK} to be finally boosted to $2V_{DD}$. As INITB changes from low to high at t_1, the proposed charge pump goes into the ordinary pumping period. Then, the main charge pump starts to pump V_{OUT} toward $2V_{DD}$ by the control of main clocks. Since V_{BULK} is already staying at $2V_{DD}$ during this period, there exists no forward bias in the source/substrate junction of all the pMOS transistors in the circuit. When V_{OUT} reaches $2V_{DD} - V_{TH}$ at t_2, the auxiliary control clocks are frozen due to the pull-down of EN_{AUX}, deactivating the bulk booster. At the same time, BSC is set to V_{DD} by the blocking control circuit (BCC), allowing ML4 and MR4 to be turned on. Any time when V_{OUT} becomes lower than $2V_{DD} - V_{TH}$ due to excessive output current (as seen in the time period between t_3 and t_4), the bulk booster is reactivated for obstructing bulk discharging to prevent bulk forward condition. Therefore, the pMOS bulk forward voltage of the proposed charge pump becomes almost zero during the entire period of charge pump operation including power-up and ordinary pumping periods. This allows the surging current to the substrate to be negligible, greatly reducing the chance of latch-up in the circuit and reducing the loss of boosting charge from the boosting nodes.

4 Simulation and comparison

To evaluate the effectiveness of the proposed scheme, the conventional [4, 5, 6] and proposed charge pumps are designed in an 80-nm CMOS process. These charge pumps have a main pumping capacitance of 20 pF and an auxiliary bulk pumping capacitance of 5 pF. The reservoir capacitances on the output and bulk nodes are 100 pF and 10 pF, respectively. HSPICE simulation is performed for these charge pumps at a supply voltage of 2.0-V with a clock frequency of 20-MHz using the parasitic model described in Section 2.

Figure 3 (a)–(d) shows the simulated waveforms for the substrate currents in CMOS charge pumps during the front several cycles in the power-up period. When Rs is 0.5 KΩ, the conventional charge pumps identically have a periodic peak substrate current over 1 mA, resulting in quite large amount of charge loss. When Rs increases to 1 KΩ, the substrate currents of the conventional charge pumps are considerably increased, making all of them eventually enter the latch-up state. On the other hand, since the amount of substrate current of the proposed charge pump is negligibly small regardless of the value of Rs, the circuit never enters the latch-up state, indicating a superior performance in terms of charge loss and latch-up immunity. Migration of pMOS bulk forward voltage of charge pumps as pumping cycle proceeds is compared in Fig. 3 (e) when Rs is equal to 0.5 KΩ. The bulk forward voltage of the conventional charge pumps becomes very high and can reach up to

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Received February 10, 2009
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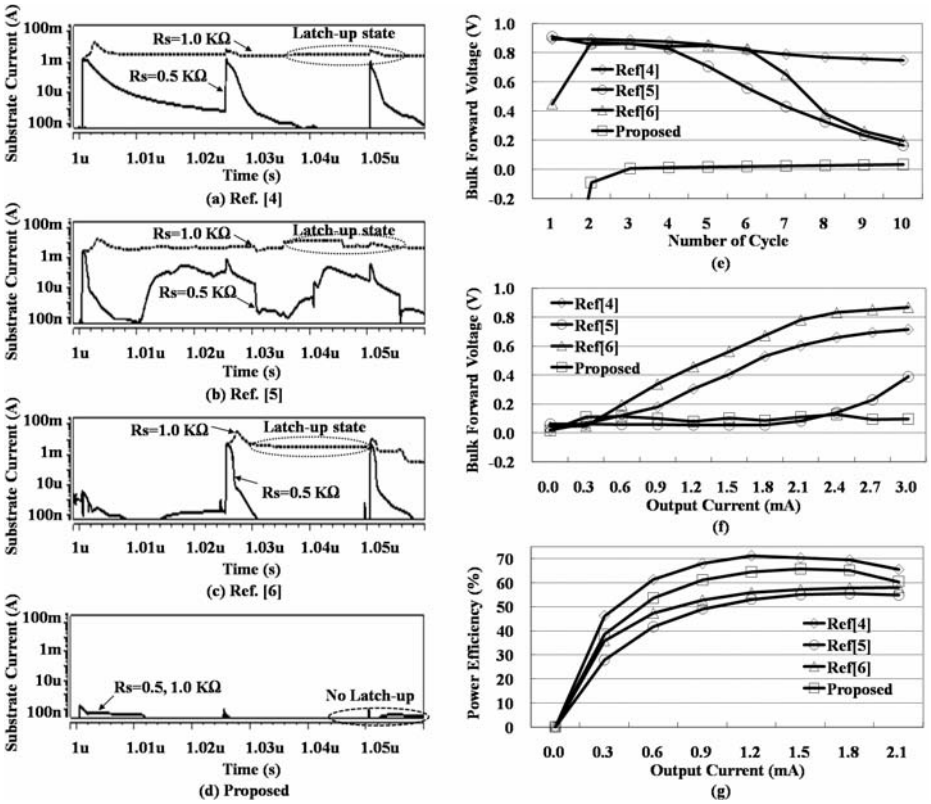

Fig. 3. (a)–(d) Simulated waveforms for substrate currents in conventional and proposed CMOS charge pumps, (e) pMOS bulk forward voltage during the first several cycles in the power-up period, (f) pMOS bulk forward voltage versus output current, (g) power efficiency versus output current.

0.9 V during the first a few cycles. On the other hand, that of the proposed charge pump is always maintained to be less than 0.05 V during the entire operating period, significantly increasing the stability. The influence of the amount of output current on the bulk forward voltage during steady-state pumping operations is depicted in Fig. 3 (f). The bulk forward voltages of the conventional charge pumps are increased in proportion to the amount of output current, indicating that they become weaker in terms of latch-up immunity as the output current increases. Meanwhile, that of the proposed charge pump is always less than 0.12 V regardless of the amount of output current, implying that the proposed circuit still retains the feature of high immunity to latch-up even for a large output current. Specifically, when the output current is 3.0 mA, the bulk forward voltage of the propose charge pump is reduced by 85%, 75% and 88% than those of the conventional charge pumps in [4, 5, 6], respectively. Fig. 3 (g) shows the simulated comparison for the power efficiency of charge pumps depending on the amount of output current. The proposed charge pump provides 10% and 8% better power efficiency than the conventional charge pumps in [5] and [6], respectively. Although the power efficiency of the proposed charge pump is slightly less than that of the conventional charge pump in [4], we should note that the

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
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performance of proposed charge pump in term of charge loss and latch-up immunity is far superior to those of conventional charge pumps.

5 Conclusion

A CMOS cross-coupled charge pump with improved latch-up immunity is presented in this paper. In the proposed charge pump, a dedicated bulk pumping and blocking (DBPB) technique is used to minimize charge loss and eliminate latch-up problem due to pMOS bulk forward. Comparison results indicate that the pMOS bulk forward voltage of the proposed charge pump is reduced by up to 88% during power-up and ordinary pumping operations regardless of the amount of output current.

DOI: 10.1587/elex.6.736
Received February 10, 2009
Accepted May 07, 2009
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