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New charge pump circuits for high output voltage and large current drivability

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Abstract: New charge pump circuits with high current drivability in low supply voltage are proposed. It generates a large gate-overdrive voltage of charge transfer MOSFET by pulling down the gate node voltage by deliberate leakage. A proper clock circuit is also presented to effectively suppress accompanied loss effects. The characteristics of the proposed charge pumps were investigated through simulation and measurement of fabricated circuit. The measurement result shows an excellent pumping performance especially under the condition of heavy load current.

Keywords: charge pump, high voltage, flash, dickson, DC-DC

Classification: Integrated circuits

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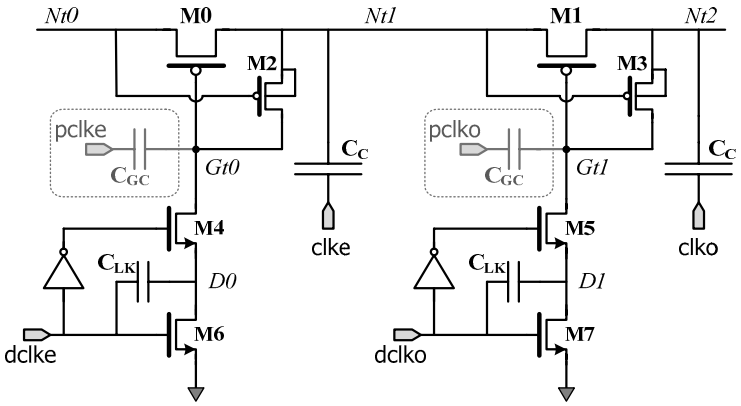
1 Introduction

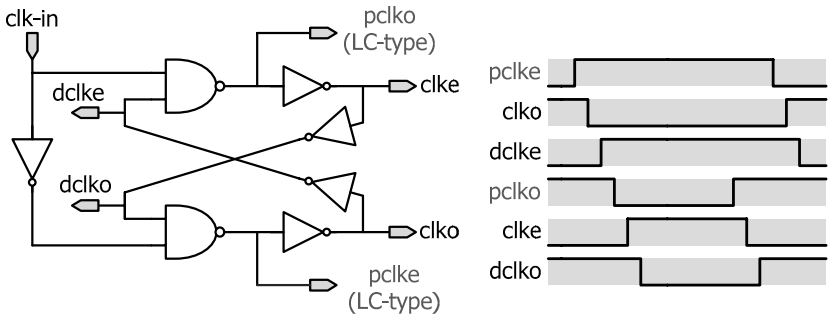
Flash memories or system-on-chip devices with flash cells require high voltage generator for the programming and the erasing operations. An important issue in those applications is high voltage generation with high current drivability in the low supply voltage. Numerous charge pump (CP) circuits, mostly based on Dickson's CP [1], have been proposed to improve voltage efficiency and current drivability [2, 3]. However, they require a differential circuit structure or the 4-phase clocks which industries may not prefer due to design burden [4]. To avoid performance degradation by body effect, many works use pMOS transistors as the charge transfer MOSFET (CTM) and have a dynamic well-bias control to the n-well [5]. The reduced mobility of pMOS, however, reduces current drivability also. In this paper we present new CP circuits with non-differential circuit structure and relatively simple clock generation, obtaining higher current drivability and suffering less loss effects even with pMOS CTM.

2 Proposed circuits

A proposed CP circuit (L-type) is shown in Fig. 1 with another slightly different version (LC-type). A new scheme of generating large gate-overdrive



(a) basic 2-stages



(b) clock circuit and phases

Fig. 1. (a) basic two (even & odd) stages of the proposed CP. The black lined comprises the L-type and the gray part in dotted boxes is included to the LC-type. The 'e' and 'o' imply even and odd phases. (b) clock circuit and the phases.

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voltage is applied, where the gate voltage of CTM (*M0*, *M1* in Fig. 1) is not coupled down by clock pulse but pulled down by leaking current when the CTM is turning on. The circuits employ the dynamic n-well biasing scheme proposed in [5].

Basic operation of the CP circuit is explained as follows, with the case of the 2nd stage in Fig. 1 (a). When the even-clock (*clke*) becomes high and the odd-clock (*clko*) becomes low, following operations take places sequentially. *M3* turns off first. *M5* turns on as *dclko* falls after *clko*. Then, *Gt1* voltage goes down, and *M1* becomes turned on so that charges transfer from *Nt1* to *Nt2* till the two node voltages are same. When *clke* becomes low and *clko* becomes high, *M3* turns on to equalize *Gt1* voltage to *Nt2* voltage so that *M1* turns off and blocks the backward flowing of charges. These operations occur at each even and odd stage in turn.

M4∼*M7* nMOS switches with C_{LK} are used to generate the leaking charge to pull down the gate voltage. As *dclko* falls, a certain amount of charge is dumped from *Gt1* node to capacitor C_{LK} until node *D1* voltage reaches $V_{DD} - V_{TN}$. The voltage drop of *Gt1* node (ΔV_G) corresponds to Eq. (1), where C_G denotes the *Gt1* node capacitance. As shown in Eq. (1), ΔV_G is independent of *Gt* node voltages and can be precisely designed by controlling C_{LK}/C_G ratio. Since C_{LK} is coupled to *dclko* instead of ground node, we can reduce C_{LK} capacitance in the low V_{DD} and prevent the through-current from *Gt* node to ground when *dclko* rises.

$$\Delta V_G = \frac{Q_{LK}}{C_G} = (2\,V_{DD} - V_{TN}) \times {}^{C_{LK}}\!/_{C_G}\,. \tag{1}$$

This leaking scheme has two benefits. It relaxes the condition of clock phases compared to the 4-phase clock schemes [2, 3]. The *dclko* fall should come after *clko* fall in order to turn on the CTM (*M*1) only after *Nt1* voltage goes higher than *Nt2*. However, *dclko* rise can occur at an arbitrary phase since it has no effect on node *Gt1*. Large gate overdrive is the other benefit. Contrary to the pseudo 4-phase CP [4], it holds the large gate overdrive voltage until the clocks turn the CTM off, leading to strong current drivability especially in the low V_{DD}.

The proposed CP, however, may have two kinds of loss effects. One is the output loss due to the leakage charge for ΔV_G. Each stage loses the charge of $\mathbf{C_G \cdot \Delta V_G}$ per clock cycle by the leakage. For an $\boldsymbol{N}$-stage CP in steady-state without load current, $\boldsymbol{K}^{\text{th}}$ stage transfers the charge of $\mathbf{(N - K + 1) \cdot C_G \cdot \Delta V_G}$ to supply the leaking charges in that stage and the following $\mathbf{(N - K)}$ stages, inducing a voltage drop of $\mathbf{(N - K + 1) \cdot \Delta V_G \cdot C_G / C_C}$ at the stage. Total loss in the output is added up as Eq. (2). Assuming $\boldsymbol{N} = 10$, $\Delta V_G = 1\,\text{V}$, and $C_G = 0.005 \cdot C_C$, V_{LOSS} is 0.275 V in total, 27.5 mV per stage. This is not a big loss. Besides, the loss is further reduced as the parasitic C_G decreases by scaled technologies.

$$V_{LOSS} = \frac{N(N+1)}{2} \cdot \Delta V_G \times {}^{C_G}\!/_{C_C}\,. \tag{2}$$

The second loss term is the adverse current which may be one of the most serious loss effects in many CPs including the pseudo 4-phase CP. In the

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proposed CP, the adverse current can arise when nodes *Nt1*, *Nt2* are coupled away from each other before the CTM turns completely off. Non-overlap clocks can diminish the loss effects to a high degree. In Fig. 1 (b) is shown the clock circuit which generates the main coupling clocks, *clke* & *clko*, and the leakage control clocks, *dclke* & *dclko*, which have the delayed fall edges for the proper switching sequence when the CTM turns on. The circuit design is simple and straightforward despite somewhat complicated look at the first glance.

Fig. 2 shows simulation waveforms of the proposed CPs. We can see the benefits of non-overlap clocks from the simulation of L-type CP in Fig. 2 (a). If *Nt1* falls before *Nt2* rises when the CTM is turning OFF, it reduces both period and magnitude of the adverse current, compared to the opposite case. If *Nt2* falls before *Nt1* rises when the CTM is turning ON, it allows *Gt1* to go down with *Nt2* as much as $\boldsymbol{\alpha}$ in Fig. 2, which lessens amount of the leakage charge required to develop ΔV_G. Both have substantial effects on the output voltage.

With all treatments, however, the L-type circuit cannot remove the adverse current completely. By adding a direct coupling capacitor (C_{GC}) to

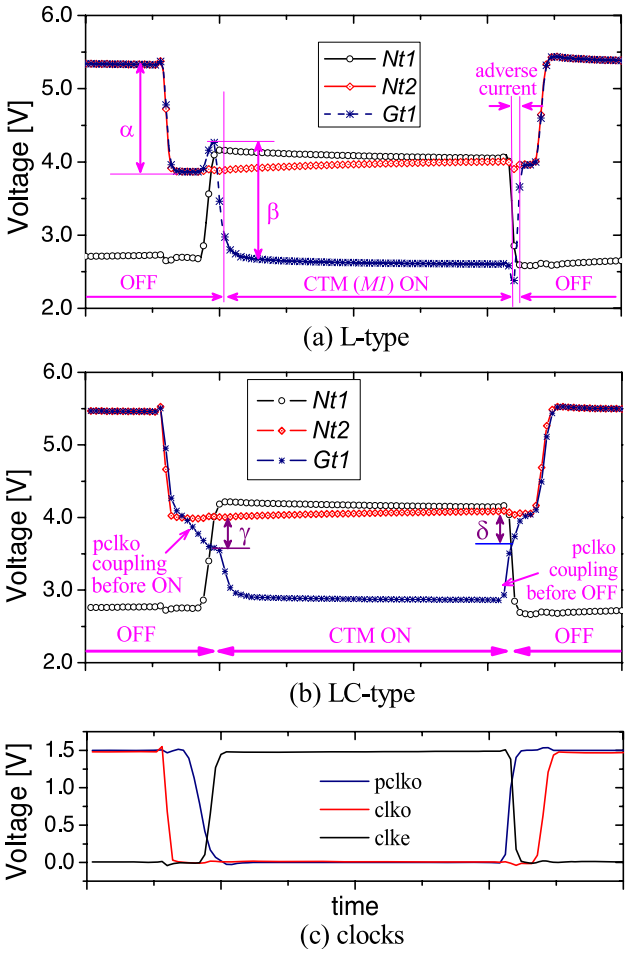

Fig. 2. Simulation waveforms of a stage of (a) the L-type and (b) the LC-type CP with the relevant clocks shown in (c)

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the *Gt* nodes (LC-type), the adverse current can be eliminated. To prevent adverse current, *M1* should be turned off before *clke* or *clko* transits, thus *pclko* rise must come before *clke* fall which precedes *clko* rise in the non-overlap clock scheme. We can pick up *pclko* from the clock circuit as shown in Fig. 1 (b) and *pclke* similarly.

We can see detailed effects of *pclk* coupling to *Gt* nodes from the simulation of LC-type CP shown in Fig. 2 (b). The *pclko* transits earliest among the clocks when the state turns from ON to OFF in Fig. 2 (b). It reduces the gate-source voltage of *M1* within V_T ($\boldsymbol{\delta}$ in Fig. 2 (b)) by kicking up *Gt1* voltage, preventing the adverse current. When the state turns from OFF to ON, *pclko* coupling may be earlier than desired. However, *Gt1* voltage is bounded within V_T from *Nt2* voltage ($\boldsymbol{\gamma}$ in Fig. 2 (b)) since *M3* is still on. The adverse current is avoided here too. However, the LC-type may demand an increased leakage charge due to the C_{GC}.

3 Simulation and measurement results

Fig. 3 (a) shows simulation results of the output voltage with various stage numbers. In this paper, the stage number is counted including the last stage which does not pump up the voltage. The proposed L-type and LC-type have output voltages a little lower than the theoretical limit, i.e. V_{DD} multiplied by the stage number N, but much higher than the pseudo 4-phase CP.

The C_{LK} value is the major design parameter of the proposed circuits.

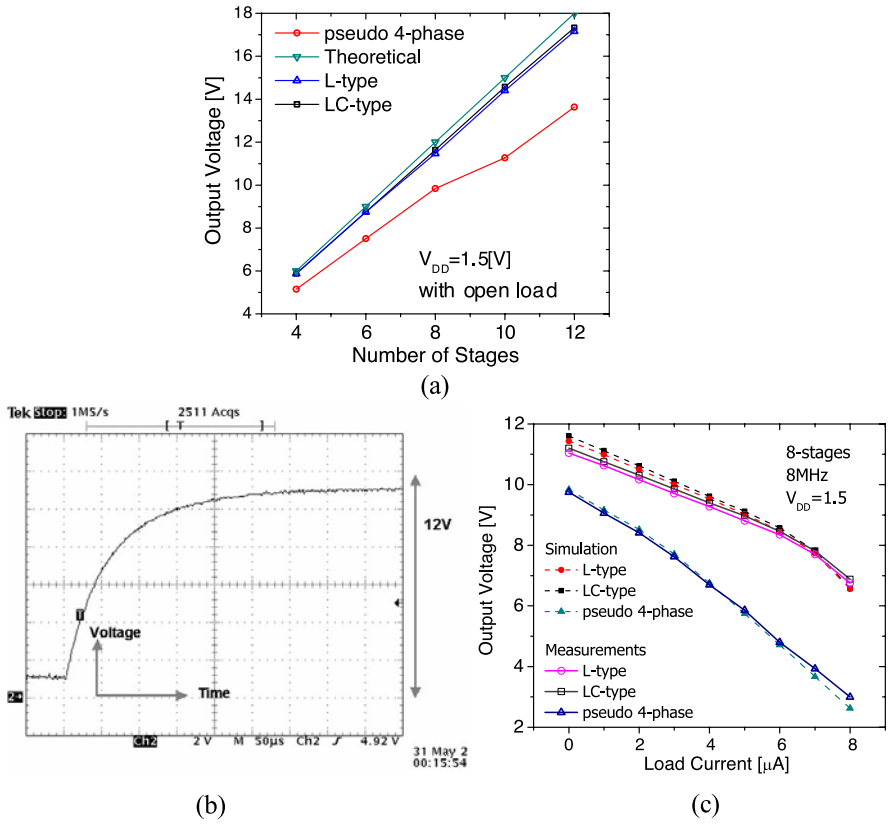

Fig. 3. Simulation and measurement results of the proposed CPs with the pseudo 4-phase CP.

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The optimized C_{LK} varies with operation conditions. Pumping performance at heavy load current is enhanced by increased C_{LK}. The merit of LC-type is that its performance is quite insensitive to the C_{LK} value compared to the L-type. Optimum values of C_{LK} and C_{GC} are far less than the capacitances used for gate coupling in the pseudo 4-phase CP, saving the layout area also.

The L-type and LC-type CPs are fabricated together with the pseudo 4-phase CP in a custom 1 μm CMOS process where very high voltage is sustained owing to 18 nm-thick gate oxide. MOS capacitors are used for the coupling capacitors, designed to have about 4 pF capacitance. A measured output waveform with 8 stages and 1.5 V V_{DD} is exhibited in Fig. 3 (b).

Measured output voltages of the fabricated charge pumps with 8 stages are plotted along the load currents in Fig. 3 (c). The proposed CPs produce much higher outputs than the pseudo 4-phase CP at open load. And the gap between the output voltages becomes wider as the load current increases, verifying excellent current drivability of the proposed CPs. The measured output voltages of the proposed CPs are a little lower than predicted by simulations at open load, which can be attributed to the effect of parasitic capacitance.

4 Conclusion

We suggested new charge pump circuits which adopt new scheme to obtain the gate-overdrive voltage by charge leaking. A non-overlap clock circuit used for the CPs is also described. Performance of the proposed CPs is investigated through simulations and verified by measurements of fabricated circuits. It shows much improved performances especially at the high load current in the low V_{DD} compared with the pseudo 4-phase CP, while maintaining simple circuit topology and design.

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