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Three-dimensional ultrasonic imaging operation using FPGA

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Abstract: The feasibility of three-dimensional (3D) ultrasound imaging methods that involve computations depends on the performance of a computing system, which requires high-speed image reconstruction. Therefore, we examine the hardware (HW) implementation of the algorithm utilizing a field-programmable-gate-array (FPGA). Subsequently, we analyze the critical path delay of the HW and reduce the delay by modifying the architecture using FPGA resources to increase the maximum frequency.

This paper presents a HW implementation approach for performing 3D ultrasound imaging.

Keywords: 3D ultrasound imaging, beamforming, FPGA, hardware

Classification: Integrated circuits

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1 Introduction

We have previously developed a 3D ultrasound imaging system involving computations for use in medical diagnostic applications [1]. In the present system, an image reconstruction algorithm is implemented in C language. When computation is performed on a personal computer (PC), the latency for generating a 3D image is approximately 40 [s/frame]. Thus, it would be difficult to perform high-speed image reconstruction by a software (SW) processing.

For practical applications, the reduction in computation time is one of the most important issues. Digital-signal-processor (DSP), graphics-processing-unit (GPU), and FPGA are mainly utilized for high-speed computation and lower cost. As the data computed in our system are fixed-point data, the system is suitable for use in FPGA [2].

This paper presents an image reconstruction algorithm and discusses the HW design and path delay analysis.

2 Image reconstruction operation for HW implementation

Image reconstruction [3] consists of the following operations in the frequency domain [4]: a beamforming by delay and sum (D&S) and a matching operation by cross-correlation.

Concept of the operation is shown in **Fig. 1**. The filters compute the cross-correlations between the received and the reference beamforms corresponding to different directions in the imaged region. Each beamform is obtained by performing the D&S on the received and reference waveforms. The procedure of the operation is as follows:

i) The reference and received waveforms ($\mathrm{N_{time}} = 2048$ [samples/ch]) are transformed using FFT into the frequency domain. Let $H_i^{(p)}(f)$ ($\mathrm{i} = 0, \ldots, (\mathrm{N_T} = 32) - 1$) and $R_j^{(p)}(f)$ ($\mathrm{j} = 0, \ldots, (\mathrm{N_R} = 32) - 1$) denote the frequency-domain description of the transmitted waveform corresponding to the i-th transmitter and that of the received waveform corresponding to the j-th receiver for a f-th data in the p-th transmission, respectively. The data length is $\mathrm{N_b} = 512$ [samples/ch].

ii) The reference beamform $B_H^{(p)}(\theta, \varphi, f)$ is computed by performing the D&S using $H_i^{(p)}(f)$ and carrying out phase rotations ($e^{-j2\pi f \tau_{\theta,\varphi,i}}$). The received waveforms are transformed into the frequency domain, and $R_j^{(p)}(f)$ for each receiver is input to the beamformer containing phase rotations ($e^{j2\pi f \tau_{\theta,\varphi,j}}$) of the receivers; subsequently, the received beamform $B_R^{(p)}(\theta, \varphi, f)$ is computed. Each beamform is represented as follows.

$$B_H^{(p)}(\theta,\varphi,f) = \sum_{i=0}^{N_T-1} H_i^{(p)}(f) e^{-j2\pi f \tau_{\theta,\varphi,i}}, \quad B_R^{(p)}(\theta,\varphi,f) = \sum_{j=0}^{N_R-1} R_j^{(p)}(f) e^{j2\pi f \tau_{\theta,\varphi,j}} \tag{1}$$

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iii) Cross-correlation is performed by matched filters and is carried out for $B_R^{(p)}(\theta,\varphi,f)$ and $B_H^{(p)}(\theta,\varphi,f)$. The filters perform the following operation.

$$\begin{aligned} s^{(p)}(\theta,\varphi,f) &= B_R^{(p)}(\theta,\varphi,f)\cdot B_H^{(p)}(\theta,\varphi,f)^* \\ &= \sum_j R_j^{(p)}(f)e^{j2\pi f\tau_{\theta,\varphi,j}}\cdot\sum_i H_i^{(p)}(f)^* e^{j2\pi f\tau_{\theta,\varphi,i}} \end{aligned} \tag{2}$$

$s^{(p)}(\theta,\varphi,f)$ denotes the output of the filter for the direction (θ,φ) for the p-th ultrasound transmission and reception cycle.

iv) The IFFT of $s^{(p)}(\theta,\varphi,f)$ is performed, the cross-correlation is consequently computed. The complex voxel series is reconstructed in the direction (θ,φ). The data output from the HW is 2048 [samples/line] $\times$ 2.

$$s^{(p)}(\theta,\varphi,t) = \Im^{-1}\left\{s^{(p)}(\theta,\varphi,f)\right\} \tag{3}$$

v) The above-mentioned operation is repeated in the imaged region for all the directions ($N_\theta \times N_\varphi = 64\times 64$).

vi) Finally, the output voxels form a 3D image. The above-mentioned operation is repeated for every ultrasound shot cycle.

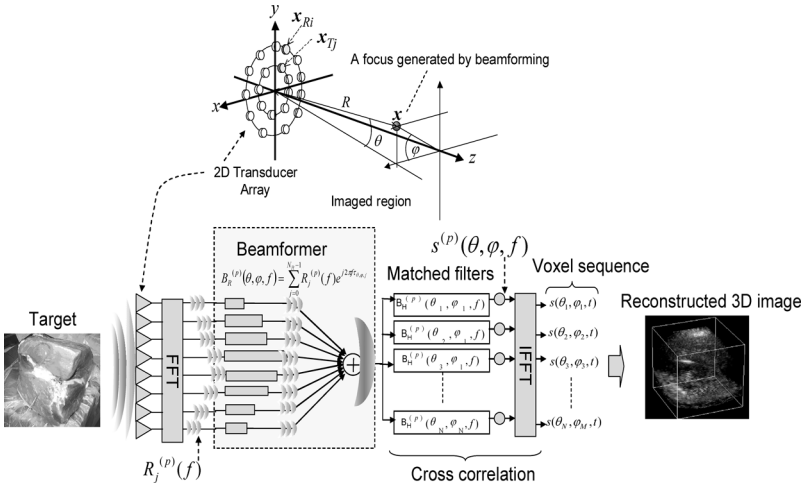

Fig. 1. Concept of image reconstruction.

3 HW design

We first map the functional blocks of the operation, (left-hand side of **Fig. 2**). The diagram represents the units required for the blocks. It additionally shows the operational flow in the HW. H-data and R-data denote reference and echo data in the frequency domain. T-data denote the delay corresponding to the distance between the focuses in the imaged region and the devices in the array. The T-data is classified into T_T- and T_R-data that denote the delays corresponding to each device. The blocks are as follows:

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FFT: The echo data obtained by ultrasound shot cycle are transformed into the frequency domain.

H-data and T-data Look-up Table (LUT): The H-data LUT contains H-data for one-shot image reconstruction and the T-data LUT contains the T-data.

D&S Beamformer: The D&S is computed with the H- and R-data. The T-data are read from the LUT and the phase rotations are computed. Subsequently, the product of the phase rotations and the waveform data is computed by a complex multiplier (CMP), and the products are then summed by a complex adder (CAD) or accumulator (ACC). Finally, the outputs of the reference and the received beamforms are generated.

Matching Operator: $s^{(p)}(\theta, \varphi, f)$ is obtained as the product of the reference and the received beamform by CMP; this product is considered as a matching operation.

IFFT: The IFFT is performed for $s^{(p)}(\theta, \varphi, f)$ to complete the cross-correlation, and the complex voxel data $s^{(p)}(\theta, \varphi, t)$ are output.

The right-hand side of **Fig. 2** shows the designed HW. The "User logic" is the HW.

The FFT and IFFT operators are implemented using Xilinx-IP; the operations are performed for every one-channel data series.

The phase rotation unit computes the phase rotation using the T-data; this is implemented by a multiplier, counter, and sin/cos table ROM [3]. The table outputs the phase rotation corresponding to the address generated by the T-data and the sampled frequency number.

The CMP and CAD are an multiplier and adder for the complex data, respectively. The CMP contains four multipliers and two adders; embedded multipliers containing in target FPGA are utilized for construct the CMP. The CMPs in the D&S beamformer compute the product of the waveform data and the phase rotation, phase adjustment of the waveform is performed. The CMP in the matching operator computes the product between the H-beam and the R-beam data. CADs are utilized to sum the multi-channel's waveform data after phase adjustment.

The ACC is used to compute the beamform data and simultaneously performs addition and data write/read by using the RAM in every clock with a wave data after phase adjustment. The ACC repeats the operation for all the channel's waveform data. The beamform data are transfered to the CMP for cross-correlation. The CMP performs the matching operation between the reference and the received beamform; the results are transferred to the IFFT operator. Consequently, complex voxel data are output.

The MicroBlaze [5] transfers the one-shot H-data series to the internal RAM in the FPGA whenever the HW completes a one-shot operation.

Here, we optimize the HW for higher-speed operations. First, we implement four operational pipelines to the each beamformer because the computational complexity of image reconstruction is determined by the D&S [3]. Moreover, we introduce two operational modes that switch the operational flow according to the action of the imaging system; at first, the HW si-

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multaneously performs the operation and the received data acquisition in the external mode when the imaging system performs ultrasound shot cycle. RAM_Es are utilized only in this mode. This mode is applied to the first line of image reconstruction. Subsequently, the HW is switched to the internal mode and the operation is performed in parallel by utilizing R-data obtained in the external mode. This mode is repeated for all the remaining directions ($(64 \times 64) - 1$ [line]). A 3D-image sequence is generated after the internal mode.

We design and synthesize the HW by utilizing Xilinx-ISE9.1.03i. Target FPGA is Xilinx- XCVFX100.

The constructed HW's maximum frequency is approximately 137 [MHz] (path delay $\fallingdotseq$ 7.3 [ns]). The latency for 3D images containing $64 \times 64 \times 256$ voxels is approximately 170 [ms/frame], the throughput is approximately 5.9 [frame/s]. The processing speed is approximately 236 times faster than that of SW.

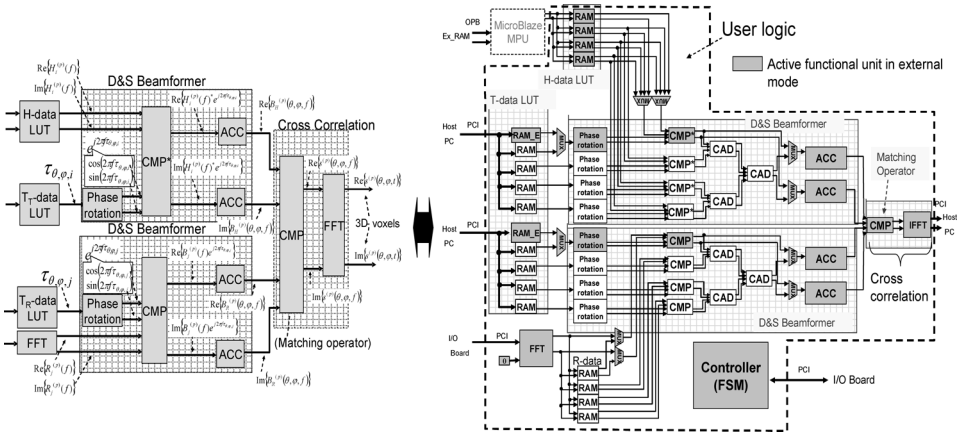

Fig. 2. Architecture mapping based on functional blocks (left-hand side) and designed architecture (right-hand side).

4 Critical path analysis and improvement

First, the HW is divided into some rough functional units. Then, we search each path delay every divided unit. Consequently, we find the critical path in the D&S beamformers. In detail, the path exists in the sin/cos table in the phase rotation unit. So, we change the table type from FPGA logic blocks to Block RAM which is memory resources in FPGA. Consequently, the path is improved. The next critical path exists on the dual port RAM in the ACC, as shown in the left-hand side of **Fig. 3**. Similarly, we modify the implementation type. The dual port RAM was implanted by the block RAM. So, we implement the ACC utilizing the shift register containing the enable signal.

Subsequently, some registers are inserted between the CMP in cross-correlation and the IFFT core, the critical path is modified. The maximum

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frequency of the improved HW is approximately 200 [MHz] (path delay ≒ 5 [ns]), and the path delay is approximately 32% smaller than that in the previous version. The latency is approximately 116 [ms/frame], and the throughput is approximately 8.6 [frame/s].

The processing speed is approximately 1.5 times faster than that of the previous HW.

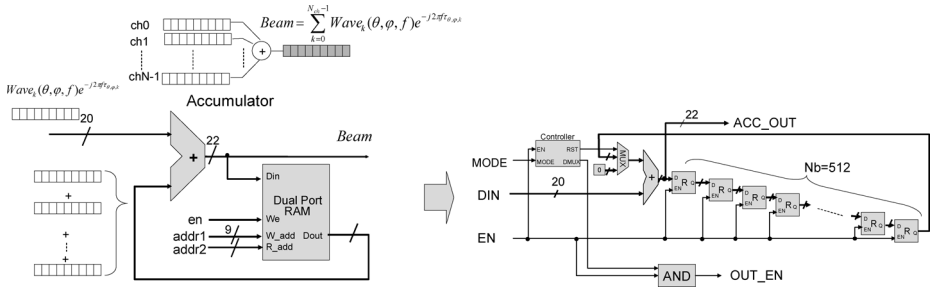

Fig. 3. Modification of architecture of the ACC using FPGA resources.

5 Conclusion

In this study, we examined HW implementation on a FPGA for high-speed computation and lower cost.

Image reconstruction is performed in the frequency domain to reduce the computational complexity of cross-correlation; The HW switches between two operational modes according to action of the imaging system.

The processing speed of HW is approximately 240 times faster than that of SW. Then the architecture modification was tried, processing speed of the modified HW was approximately 1.5 times faster than that of the previous version.

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