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Piecewise linear-in-dB variable gain amplifier to enhance integral nonlinearity

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Abstract: A new technique to improve the integral nonlinearity of the "linear-in-dB" variable gain amplifier (VGA) by adopting a piecewise linear transfer curve rather than a single curve is presented. The conventional single curve which is the first-order approximation of the exponential function yields bigger deviation errors as the gain control code advances. The integral nonlinearity (INL) of the proposed piecewise linear curve can be managed to be smaller because one of divisional curves moves to another before the deviation becomes prominent. A generic circuit schematic without chip size overhead is suggested with its future expansion in mind, and a design in a 0.35 μm CMOS process under 3.3 V supply is proposed and verified.

Keywords: linear-in-dB VGA, variable gain amplifier, CCD, analog front end

Classification: Integrated circuits

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1 Introduction

Charge-coupled device (CCD) image sensors need an analog-front-end (AFE) and an image signal processing (ISP) units. Particularly, the AFE is critical in determining the system performance. The VGA is an essential part in AFE, needed to realize an exponential (linear-in-dB) shaping.

A CMOS linear-in-dB VGA of the current divider type for CDMA systems [1], and an accurate switched-capacitor (SC) type linear-in-dB VGA for image sense systems were reported [2]. A possible implementation in the SC type VGA utilizes the 1st-order approximation of the exponential function [3]. The conventional CMOS linear-in-dB VGA uses a single curve for the implementation, which can achieve a gain from 0 to 6 dB by 0.094 dB step (8 bit resolution from 0 to 24 dB) [2]. By the way, the recent CCD systems tend to require a more sophisticated gain control [4], looking for a new topology.

In this paper, a new topology of SC type linear-in-dB VGA to enhance INL without chip size overhead is proposed. A typical implementation of the topology is suggested and its performance results are described.

2 Circuit concept for piecewise "linear-in-dB" gain curve

Fig. 1 (a) depicts the circuit diagram of the proposed piecewise-linear-in-dB VGA (P-VGA). It basically adopts the conventional single-curve architecture [2], except that the reference capacitor (C_a) which is supposed to be fixed is varied in the sectionalized code ranges. During the sampling phase (φ_1), the reference capacitor C_a and the variable capacitor C_x sample the differential input signal, V_{in}^{+} and V_{in}^{-}, and C_i samples the offset voltage of the op-amp. During the hold phase (φ_2), C_a and C_x are connected to the output nodes, V_{out}^{+} and V_{out}^{-}, with the offset compensated, forming a negative feedback path of C_a and a positive feedback path of C_x. The early phase (φ_{1e}), which falls faster than φ_1, is necessarily used for the feedback switches to prevent the input-dependent charge injection error.

The SC type linear-in-dB VGA has an exponential gain control with a fine step by utilizing the first-order approximation:

$$e^{2x} \approx \frac{1+x}{1-x}, \tag{1}$$

where the variable 'x' denotes the capacitor ratio C_x/C_a [3].

The reference capacitor C_a consists of three capacitors, the basic capacitor C_{a0}, and the shaping capacitors C_{a1} and C_{a2} which are much smaller than C_{a0}. Yet, the total capacitance of C_a can remain equal to the conventional VGA.

The variable capacitor C_x, one example of which can be implemented as shown in Fig. 1 (b), increases as the code advances. It consists of binary weighted capacitors and a termination capacitor, and switches controlled by the control bits (from b_0 to b_7) from the ISP unit. It follows that

$$C_x = \sum_{i=0}^{6} b_i \cdot 2^{i-3} C_u + b_7 \cdot (5.5 C_u) \tag{2}$$

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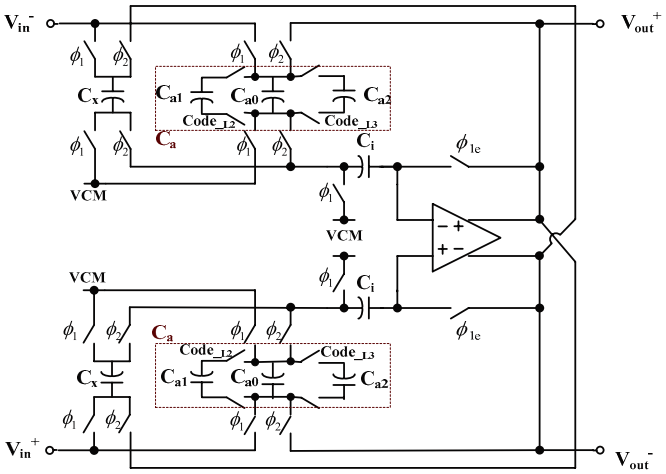

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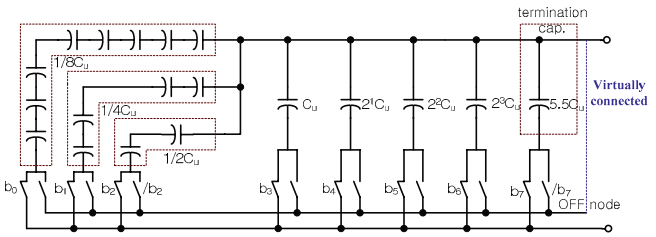

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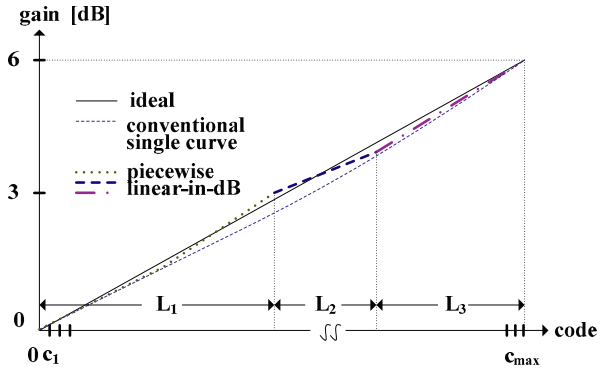

(c)

Fig. 1. Proposed P-VGA: (a) circuit schematic, (b) array of C_x with unit capacitors and switches (the reset switches in $(1/8)C_u$, $(1/4)C_u$, $(1/2)C_u$ are not shown here), and (c) comparative conceptual gain curves.

where C_u is the unit capacitance. As shown in Fig. 1 (b), the $(1/8)C_u$, $(1/4)C_u$, and $(1/2)C_u$ are implemented in a series-connection of unit capacitors. The scheme reduces the total number of unit capacitors in C_a which scales down in conjunction with the maximum value of C_x. In order to ensure the reset of capacitors when they are not selected, each unit capacitor in the $(1/8)C_u$, $(1/4)C_u$, and $(1/2)C_u$, has its own reset switch which is not shown here for simplicity.

Reduction of C_a is preferable for high-speed operation, nonetheless de-

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grades kT/C noise and capacitor mismatches. The gain of code "k" spoiled by random capacitance mismatches can be represented as [5]

$$G_k \approx G_{ideal} \cdot \Delta G\,(\delta_1/C_a, \delta_2/C_a, \cdots \delta_n/C_a) \tag{3}$$

where δ_i denotes a random mismatch error of a unit capacitor in C_x. Moreover, ΔG is increasing as the sum of $(\delta_1, \delta_2, \cdots, \delta_n)$ over C_a increases and becomes 1 if there is no mismatch. Since smaller C_a causes larger mismatch error as expressed in Eq. (3), a lower bound of the total capacitance C_a should be established.

To vary C_x given by Eq. (2), the capacitors should be connected (ON) or disconnected (OFF) depending on the control bits. When the OFF switches turn on, the parasitic capacitances in conjunction with MOS switches corrupt the charge conservation, resulting in a several milli-volt error. To mitigate the substantial signal-dependent error, the capacitor nodes are virtually equalized as illustrated in Fig. 1 (b).

Eq. (1) indicates that the larger 'x' results in the larger deviation from the exponential function. Therefore, the approximation shows the substantial limitation in the application of 0.035 dB step for the $0 \sim 6$ dB gain range.

To alleviate the difficulty, the proposed P-VGA employs three different divisional curves, in L_1, L_2 and L_3 code ranges. For the circuit configuration of Fig. 1 (a), $C_a = C_{a0}$ in L_1, $C_a = C_{a0} + C_{a1}$ in L_2, and $C_a = C_{a0} + C_{a2}$ in L_3. A different value of C_a results in the different gain slope by Eq. (1). Thus, varying the reference capacitor C_a for each range achieves piecewise-linear curves. As illustrated in Fig. 1 (c), the code ranges (L_1, L_2, L_3) are defined such that one curve is supposed to move to another before the accumulated error becomes prominent.

The appropriate value of the reference capacitance for each range can be found by a heuristic method where a number of iterative calculations of the INL and DNL are performed.

3 Design and simulation results

The proposed P-VGA is designed in a 0.35 μm CMOS process with 3.3 V supply.

The "linear-in-dB" shape from 0 to 6 dB is implemented by 0.035-dB step (1 LSB), that is, the 10-bit resolution for the overall gain control from 0 to 36 dB.

To change the gain from 0 to 6 dB by 0.035-dB step, C_x should be varied from 0 to approximately $(1/3)C_a$ by $(1/171)C_a$ step, given by Eq. (1). And hence, the last code, c_{max}, is 171. In the circuit of Fig. 1 (b), C_x is designed to be varied from 0 to $(21.375)C_u$ by Eq. (2). C_a is supposed to be $(64.125)C_u$, resulting in the overall gain of 6.02 dB, thereby actually $(64.25)C_u$ was used for the 6 dB gain.

In the proposed design, for the reference capacitors in the schematic of Fig. 1 (a), C_{a0} is set to be $(63.25)C_u$, $C_{a1} = 0$, and $C_{a2} = 1C_u$. In the L_1 region, C_a is designed to be $C_{a0} = 63.25C_u$, disconnecting C_{a2}. The last

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code of L_1 is set to be 153. The codes in L_2 are 154 and 155. The gain at the codes in L_2 remains constant from the last code of L_1, maintaining C_a, and C_x unchanged. This procedure brings about the minimum capacitor overhead, yet assures the monotonicity of the gain curve. In the L_3 region, C_a is changed to be $(64.25)C_u$, while connecting C_{a2}. Then, the divisional transfer curve in L_3 is equal to the conventional single curve. The unit capacitance C_u was chosen to be 60 fF in the process.

Note that the negative feedback factor in Fig. 1 (a), β_n, is $C_a/(C_a + C_x)$, and the positive feedback factor, β_p, is $C_x/(C_a + C_x)$ if the series-connection of C_i and the input capacitance are neglected. Since the maximum value of C_x is $(1/3)C_a$, and hence β_p is less than β_n, the overall negative feedback is ensured. The total feedback factor, β, is then $(C_a - C_x)/(C_a + C_x)$ and thereby β_{min} is 1/2.

The output referred kT/C noise can be written as

$$\overline{V}^2 = 2\frac{kT}{C_a + C_x} \cdot \left(\frac{C_a + C_x}{C_a - C_x}\right)^2 = 2\frac{kT\,(C_a + C_x)}{(C_a - C_x)^2} < \frac{V_{LSB}^2}{12} \tag{4}$$

where $V_{LSB} = 1.95$ mV for a 2 V differential swing. According to Eq. (4), it can be shown that the $C_a + C_x$ should be greater than 100 fF with β_{min} of 1/2. As C_a is 3.855 pF, the design limitation is well satisfied. The factor of 2 in the equation comes from the differential scheme, which leads to only odd-order distortion.

The noise during the amplification mode is neglected because the noise power out of the closed-loop bandwidth is suppressed. Complementary switches are used in the whole circuit to obtain moderately constant on-resistance.

Noting that the static settling error with the DC open-loop gain of A is approximated as $1/(\beta A)$, the calculation shows that the op-amp gain with β_{min} of 1/2 should be larger than 65 dB for the 10-bit accuracy. The dynamic settling error and the residual offset requires about 6-dB more gain. Taking the parasitic capacitances into consideration, a fully differential telescopic op-amp with a SC common-mode feedback scheme is selected. Using a tail current of about 2 mA, the simulated DC gain of the op-amp is about 73 dB, and the unit-gain bandwidth is 260 MHz at a load capacitance of 5 pF. The bandwidth specification is good enough to process the signal data rate of 15 MHz from the CCD sensor.

The whole circuits are implemented in the transistor level. The Spectre simulation results of the gain transfer curves are plotted in Fig. 2 (a), showing the deviations from the ideal straight line. The P-VGA shows three divisional curves where the magnitude of the gain in L_1 is closer to the ideal line than the conventional curve, the slope of the gain in L_2 is zero, and the divisional curve in L_3 is equivalent to the conventional single curve.

In Fig. 2 (b) and (c), the INL of the P-VGA is compared with that of the conventional single-curve VGA where C_{a0} and C_{a2} are connected, thus $C_a = (64.25)C_u$ is fixed over the whole range. The INL of the P-VGA is shown to be 1.5 LSB, while that of the conventional VGA is 2.94 LSB. The

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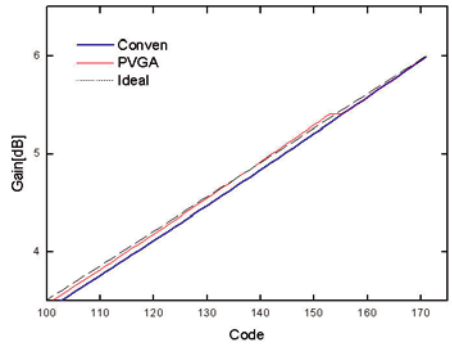

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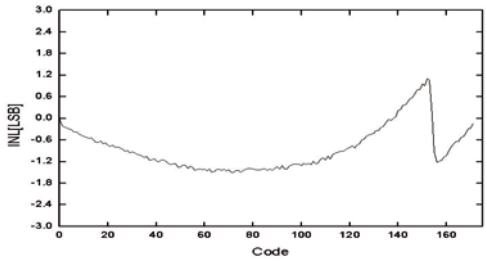

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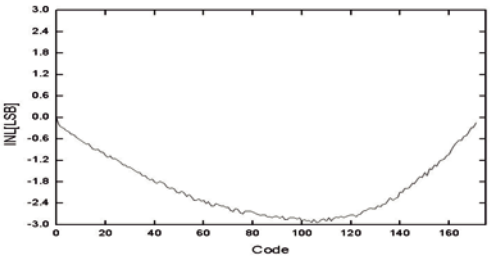

(c)

Fig. 2. Spectre simulation results: (a) detailed gain transfer curves from code 100 to 171 where the curve shows zero slope at 154 and 155 and overlaps the conventional curve from 156 to 171, and integral nonlinearities of (b) P-VGA and (c) single-curve VGA.

Table I. Performance summary of the designed P-VGA.

Parameter	Value [unit]
VGA gain range	0 ~ 6 [dB]
VGA gain step	0.035 [dB]
Linearity (INL, DNL), 1 LSB = 0.035 dB	1.5 [LSB], 1.0 [LSB]
Capacitance overhead	0 [%]
Technology	0.35 [μm] CMOS
Supply Voltage	3.3 [V]
Power Consumption	6.6 [mW]

DNL is worst in L_2, but it can be improved if the slope in L_2 is enhanced rather than zero.

The performance of the P-VGA is summarized in Table I.

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4 Conclusion

A piecewise-linear technology adopted in the "linear-in-dB" variable-gain amplifier (VGA) is presented to manage the INL more elaborately than the conventional single-curve approximation. To reduce the substantial INL by the 1st-order approximation, a method of resetting the accumulated error by using multiple gain curves is exploited. The proposed various gain curves are achieved just by varying the reference capacitance in the switched-capacitor (SC) implementation without capacitor overhead. That stands for the expandability for the more elaborate gain control. The proposed VGA in a 0.35-μm CMOS process under 3.3 V supply improves INL by 1.5 LSB than the prior art in the 0.035 dB step (10-bit resolution in $0 \sim 36$ dB gain). Applied to a wider "linear-in-dB" range (more than 6 dB gain), it would be utilized with greater benefits.

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