IEICE Electronics Express, Vol.7, No.18, 1335–1341

FPGA-based PWM for three-phase SEPIC rectifier

Siti Rohani S. Raihan[a)] **and Nasrudin Abd. Rahim**

Centre of Research for Power Electronics, Drives, Automation & Control, Level 4 Engineering Tower, Faculty of Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia

a) *srohani_sr@um.edu.my*

Abstract: This paper presents the design and implementation of synchronous pulse-width modulation (PWM) for a three-phase three-switch Single Ended Primary Inductance Converter (SEPIC). The PWM switching patterns are generated from an Altera Cyclone II field programmable gate array (FPGA) device. Two types of carrier waveforms are used with two 60^o sine waveforms, taking less space in the FPGA, providing more space for control circuits. Comparative study of two PWM methods is also shown. Verification of simulation results are based on hardware-in-the-loop technique, to show the effectiveness of digital-based PWM control.

Keywords: pulse-width modulation, FPGA, rectifier, SEPIC, hardware-in-the-loop

Classification: Science and engineering for electronics

References

[1] R. Itoh and K. Ishizaka, "Three-phase flyback AC-DC converter with sinusoidal supply currents," *IEE Proceedings-B.*, pp. 143–151, 1991.

[2] B. T. Ooi, J. W. Dixon, A. B. Kulkarni, and M. Nishimoto, "An integrated AC drive system using a controlled current PWM rectifier-inverter link," *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 64–71, 1988.

[3] K. Inagaki, T. Furuhashi, A. Ishiguro, M. Ishida, and S. Okuma, "A new PWM control method for AC to DC converters with high-frequency transformer isolation," *IEEE Trans. Ind. Appl.*, vol. 29, no. 3, pp. 486–492, 1993.

[4] V. Vlatkovic and D. Borojevic, "Digital-signal-processor-based control of three-phase space vector modulated converters," *IEEE Trans. Ind. Electron.*, vol. 41, no. 3, pp. 326–332, 1994.

[5] J. W. Dixon, "Three-phase Controlled Rectifier," *Power Electronics Handbook*, 2nd ed. M. H. Rashid, Elsevier, Inc., San Diego, pp. 123–456, 2007.

[6] V. G. Agelidis, P. D. Ziogas, and G. Joos, "Dead-band PWM switching patterns," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 522–531, 1996.

[7] N. A. Rahim, Z. Islam, and S. R. S. Raihan, "FPGA-based PWM control of Hybrid Single-phase Active Power Filter for Harmonic Compensation," *J. Scientific and Ind. Research*, vol. 69, pp. 55–61, Jan. 2010.

[8] A. M. Omar, N. A. Rahim, and S. Mekhilef, "Three-phase Synchronous PWM for Flyback Converter With Power-Factor Correction Using FPGA ASIC Design," *IEEE Trans. Ind. Electron.*, vol. 51, no. 1, pp. 96–106, 2004.

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

[9] U. Kamnarn and V. Chunkag, "Analysis and Design of a Modular Three-Phase AC-to-DC Converter Using CUK Rectifier Module With Nearly Unity Power Factor and Fast Dynamic Response," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 2000–2012, 2009.
[10] A. Fratta, G. Griffero, and S. Nieddu, "Comparative analysis among DSP and FPGA-based control capabilities in PWM power converters," *30th Annual Conf. IEEE Ind. Electronics Society*, Busan, Korea, pp. 257–262, Nov. 2004.
[11] S. Takamatsu, E. Shimada, and T. Yokoyama, "Digital Control Method for Single Phase Utility Interactive Inverter Using Deadbeat Control with FPGA Based Hardware Controller," *12th International Power Electronics and Motion Control Conference*, Portoroz, Slovenia, pp. 1436–1441, 2006.

1 Introduction

Pulse-width modulation (PWM) is a well-known wave-shaping technique for power electronic converter. Its wide range of applications invites interest to its research. Generally, most of the research is focused on optimizing PWM switching pattern. PWM schemes that have been reported include sinusoidal PWM (SPWM), hysteresis PWM, space-vector modulation (SVM), and optimal PWM [1, 2, 3, 4, 5, 6, 7]. Some schemes suit specific converter topologies only, unsuitable for others [8, 9]. PWM was designed to reduce the switching-caused low-order harmonics in a system and the switching stress on power switching devices; the low-order harmonic components are centralized at the carrier waveform's higher frequencies and their multiples so they can be easily filtered [6].

Conventionally, six switches form a controlled rectifier. The topology requires many switches, and its control is complicated (especially the dead-time required between the top and the bottom switches on each leg of the converter). Six driver circuits with six signal patterns drive the power switching devices, lessening reliability and introducing major losses through the switches' switching and conduction [5].

Integration of field programmable gate array (FPGA) technology into power converters allows very-high-speed calculation compared with a DSP-based controller, which has limited A/D conversion time and calculation time [10]. Parallel-processing control circuit can be realized in FPGA-based hardware, thus all circuits (calculation, reference generation, PLL-feedback control, and pulse-pattern generation) can be implemented in one FPGA chip, which compared with a DSP-based software controller, dramatically reduces total calculation time [11].

Here, a modified SPWM is compared with the PWM method proposed in [8], whose mode of operation, either two switches are closed at the same time or all of the switches are open at the same time, requires extra diodes to act as freewheeling path, thus reducing the efficiency of the converter. The modified SPWM is then implemented into an FPGA. For verification of the simulation results, the method is tested through simulation in

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

Matlab/Simulink and hardware-in-the-loop (HIL) technique through DSP Builder.

2 PWM design and implementation

The proposed PWM circuit is suitable for the three-phase three-switch AC/DC Single Ended Primary Inductance Converter (SEPIC) shown in Fig. 1(a). The rectifier contains power semiconductor devices that act as

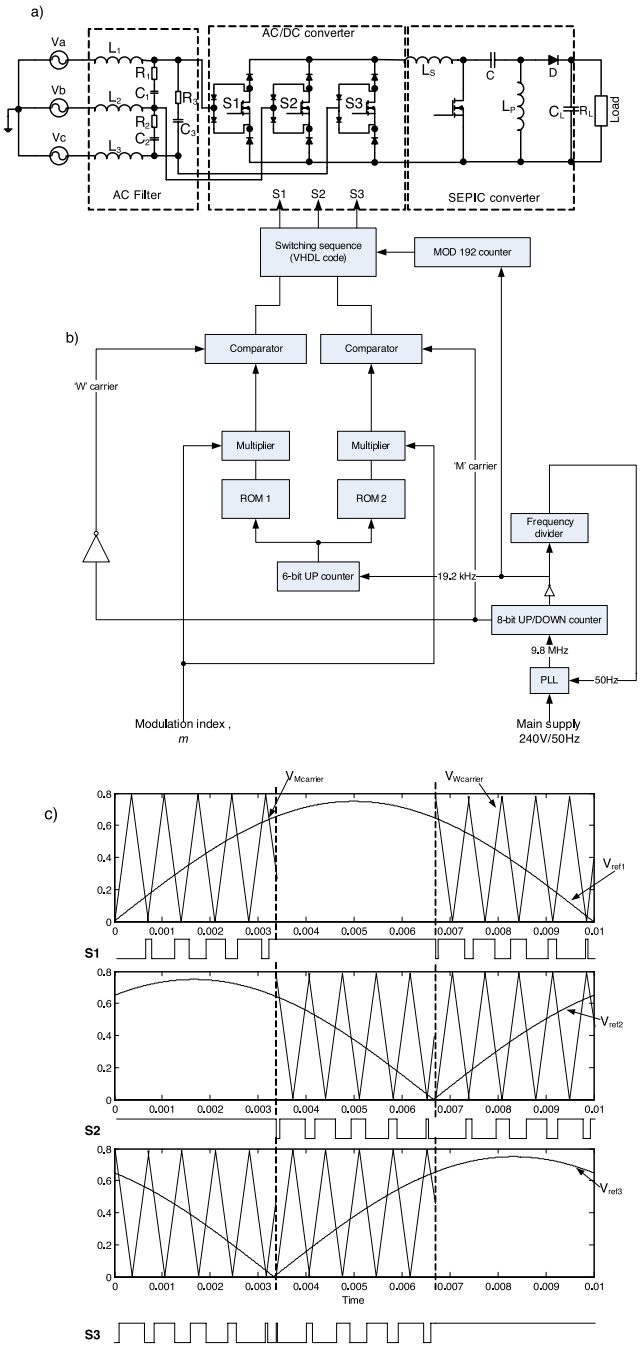

Fig. 1. a) Three-phase three-switch SEPIC converter, b) Block diagram of a synchronous FPGA-based PWM generator, c) Switching patterns for three-phase AC/DC converter.

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

switches (S1, S2, and S3) when activated by the PWM circuit's switching signal.

Fig. 1(b) shows the design of PWM circuit in FPGA. Three PWM patterns will be generated for the three switches in the AC/DC converter. The multiplier will multiply the sine data in the look-up table with the modulation index, m, which is the ratio of the amplitude of modulating signal and carrier signal.

The reference sinusoidal waveform is phase-locked to the 50 Hz AC-line for synchronization. The modulating frequency of the bridge and the line frequency are synchronized when the clock frequency and the mains frequency are locked, so, there is no mains-capture and synchronization problem as the mains supply frequency fluctuation tolerance is ±2%.

The sinusoidal waveform uses two 60° look-up tables, whose 64 sampled data are 0° – 60° and 120° – 180°. A 6-bit binary counter acts as memory pointer to the data's ROM address and the sine-wave samples are updated by clocking the counter.

3 Carrier signal

The triangular carrier is generated digitally by using an UP/DOWN counter. When the counter starts counting up and reaches maximum value, some logic gates will generate a LOW signal, indicating the counter to count down. Similarly, when the counter reaches minimum value, monitoring logics interrupt counting by producing a HIGH signal, the counter changes its counting direction, and the processes repeat.

The counter is clocked by a clock generated by the external PLL. Although Altera Cyclone II FPGA is equipped with an internal PLL, the lowest frequency it can generate is 10 MHz, which is slightly higher than the proposed design required clock frequency (9.8 MHz). The 192 sampled data will not be symmetrically synchronized with the 192 carrier waves in half-cycle time (0.01 s).

The relationship between the carrier frequency and the main clock frequency is

$$f_c = \frac{f_{clk}}{(2^n - 1) \cdot 2} \tag{1}$$

where f_c is the carrier frequency, f_{clk} is the main clock frequency generated from the PLL, and n is the number of bits of the UP/DOWN counter. The carrier wave's amplitude is fixed at 255 while the modulating wave's amplitude is varied by multiplying the look-up table data with the modulation index.

To ensure non-simultaneous conduction of the three switches, two types of carriers are used: W-shaped and M-shaped. The phase waveform's half cycle is divided into three 60° sectors. The first sector (0° – 60°) of the first reference waveform (V_{ref1}) is compared with the M-shaped carrier, while the third sector (120° – 180°) is compared with the W-shaped carrier. The second sector (60° – 120°) is fixed at HIGH so that only one switch acts as a

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

freewheeling path during this interval. Fig. 1(c) shows the switching patterns produced by switches S1, S2, and S3.

4 Hardware and software co-simulation

Conventional software-based simulation does not consider the FPGA chip's resolution limit. The software requires the design to be compiled and synthesized before being downloaded onto the device for verification. Designing the system is thus time consuming and costly. Altera DSP Builder allows integration of high-level algorithm and very-high-speed hardware descriptive language (VHDL), simulation, and verification of the circuit design in a Matlab/Simulink environment. The Simulink blocks are combined with Altera library blocks to create a circuit design that can be simulated.

In HIL system, the Signal Compiler block generates the HDL code, synthesizing and fitting the design through Quartus II within Simulink. The HIL block allows the circuit design to be programmed into the FPGA, for hardware and software co-simulation, and for reconfiguration, so risk of damaging the controller during actual testing can be reduced.

For this design, the signals are converted into fixed-point system with single-tasking mode for sampling time of 102 ns. The HIL operates in burst mode to speed-up operation, so, a latency of 1024 bits is introduced at the outputs.

5 Results

Table I shows the comparative results between the PWM scheme proposed by [8] and the modified PWM implemented in this paper. The modulation index was 0.8. The addition of extra diodes as freewheeling path reduces the efficiency and increases the THD of the SEPIC converter. The modified PWM utilizing one semiconductor switch to act as freewheeling path instead of using additional diode provides better performance compared to others.

Table I. Comparison between two PWM methods implemented on SEPIC converter.

		Power factor	Efficiency	THD (%)
PWM scheme by [8]	without freewheeling diode	0.876	0.099214	50.00
	with freewheeling diode	0.997	0.852944	3.69
Modified PWM	without freewheeling diode	0.997	0.878055	2.80
	with freewheeling diode	0.997	0.873824	5.16

When implemented into the FPGA, the modified PWM circuit uses less than 1% of the total memory and logic elements. Fig. 2 compares the simulation of the three-phase SEPIC converter with its HIL results. Figs. 2(a) and (b) show the generated PWM waveforms. The phase shift between the voltage and current signals in Figs. 2(c) and (d) is near zero, thus the power factor is near unity for both. The effect of the actual FPGA controller on

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

the system caused the THD calculated from HIL simulation to be 3.45%, compared with the simulation's 2.8%. Due to high load voltage and current produced in the HIL-based result (Figs. 2(e) and (f)), the efficiency is 92.6% compared with 88.8% of the simulation result. Without a proper controller, Figs. 2(g) and (h) show there is an overshoot and ripple in the three-phase current.

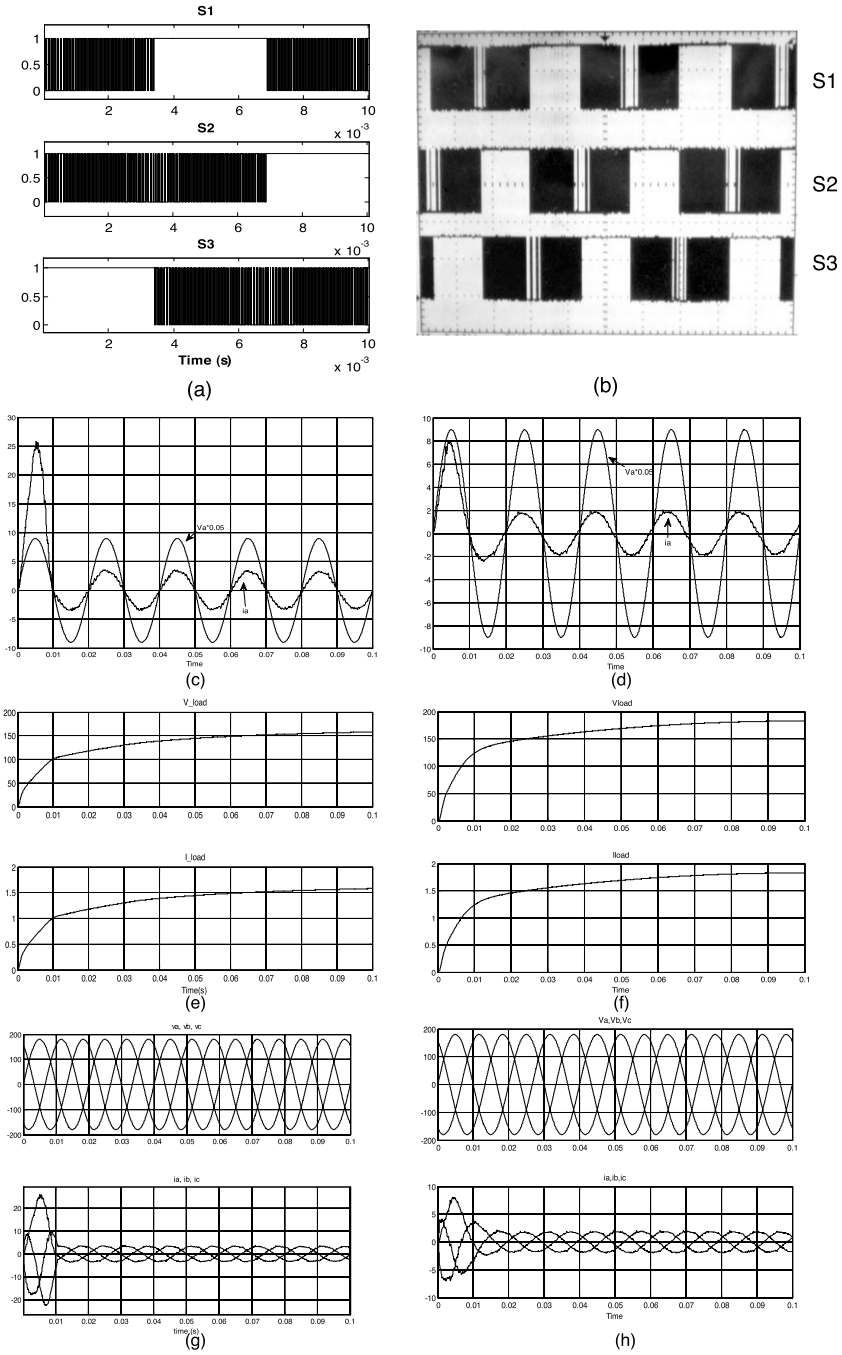

Fig. 2. Simulation results are on the left side and HIL-based results are on the right. (a) and (b): PWM waveforms for three switches, (c) and (d): Current and voltage inputs, (e) and (f): DC voltage and current at the load, (g) and (h): three-phase voltage and current.

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010

6 Conclusion

This paper presents the design for an FPGA-based synchronous PWM suited to a three-switch three-phase SEPIC converter. Experiment results based on reconfigurable HIL verified the simulation results satisfactorily. Controllers can be added into the FPGA to reduce the overshoot of the current input and the current ripple as well as the THD. HIL system provides an efficient method for modeling, simulation, and verification of the design without significant hardware modification.

DOI: 10.1587/elex.7.1335
Received April 20, 2010
Accepted August 30, 2010
Published September 25, 2010