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Fully digital clock frequency doubler

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Abstract: This paper presents a clock frequency doubler, having the function of automatic adjustable duty cycle without feedback loops. The duty cycle amount can be automatically adjustable using digitized delay block and a counter. This simplifies the design structure and allows the circuit to operate over a wide range of input frequency variation. The simulation results show that this frequency doubler operates at a very wide variable input frequency ranging from 650 MHz to 1.25 GHz.

Keywords: clock frequency doubler, digitized delay, quarter phase

Classification: Integrated circuits

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1 Introduction

The clock frequency doubler has become a commonly used component in digital CMOS systems. It can be constructed utilizing PLL, DLL with RS flip-flops [1] or other units with XOR gates [2, 3, 4] and [5]. A tunable charge pump and feedback scheme has been used in [3]. A small analog potion has been composed of a current reference [4]. In [5], a bipolar comparator circuit and passive RC integrator have been utilized.

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The robustness of the circuit becomes one of the most important features in the design of a clock frequency doubler as the PVT (Process Voltage Temperature) variation becomes more severe. To achieve the circuit's reliability and robust structure, we have implemented the clock frequency doubler with fully digital circuits. Every circuit of the proposed clock frequency doubler consists of digital logic gates. Charge sensing block that is usually composed of analog circuit, as in [4], is also implemented with digital logic gates in our design. Furthermore, to eliminate the balancing error, a new reset mechanism is designed to perform the reset operation on every clock cycle. The critical path delay of the proposed clock frequency doubler has been measured with 800 ps on the 0.13 um Samsung process, so that it can support up to 2.5 GHz. This is because the clock frequency doubler can generate a clock frequency two times faster than its own operating frequency. In the virtue of the digital circuit structure, design time and effort is much less than those of the analog based design.

2 Implementation

Fig. 1 presents the block and timing diagrams of the proposed fully digital clock frequency doubler. Once the delayed clock (CLKD) signal is produced with a quarter phase delay for the input clock, twice of the input clock frequency is generated on the CLKX2 output port in the XOR gate operation. This circuit is operated in following steps. First, the CLKD signal is produced by delaying the CLK through the digitized delay block whose delay is controlled by up-down counter. Second, in the quarter-phase detector,

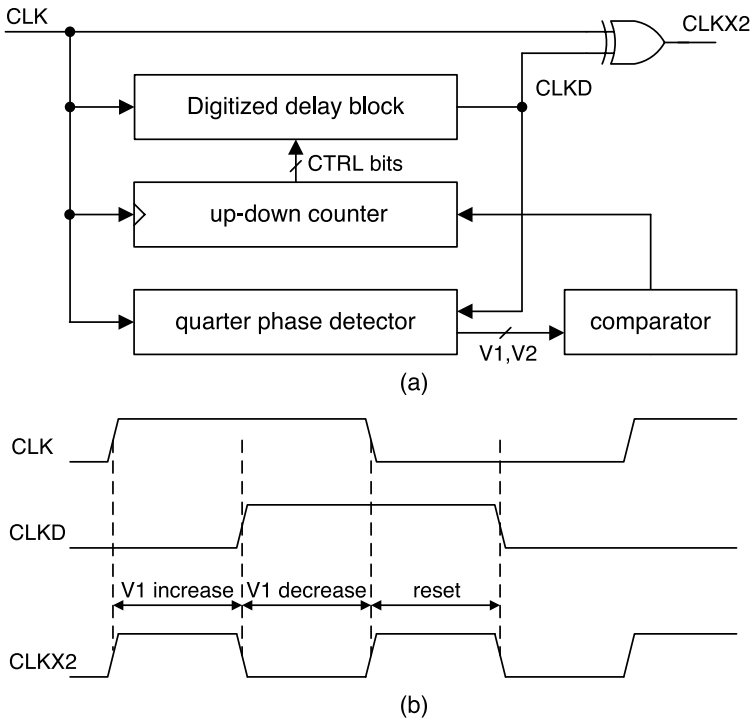

Fig. 1. Overall clock frequency doubler diagrams. (a) Block diagram, (b) Timing operation diagram

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the capacitor is charged in the V1-increase period and discharged in the V1-decrease period as shown in the waveform of Fig. 1 (b). The final voltage level is compared with the reference voltage, V2. Third, the voltage difference is detected by a comparator that is constructed by a two-stage differential amplifier to generate logic one or zero signals. Finally, the generated logic signal is delivered to up-down counter in order to decide to increase or decrease steps of the digitized delay. Following subsections explain the operation of major components in detail.

2.1 Digitized delay block

The digitized delay block is composed of delay element chains and a delay controller as shown in Fig. 2 (a) and Fig. 2 (b). The delay element chain composed of four delay elements receives an input clock signal from the port "in" shown in Fig. 2 (a) and generates a delayed clock as an output to the port "out". The delay controller adjusts the amount of delay based on the input value. The input of the delay controller consists of four-bit binary digits to provide the delay amount of sixteen levels. Fig. 2 (c) shows the detail structure of a delay element. The PMOS and NMOS transistors have four different widths and are parallel connected in the delay element. The delay element generates appropriate delayed clock signal through activating one of the four P/NMOS transistor pairs based on the control signal delivered from the delay controller.

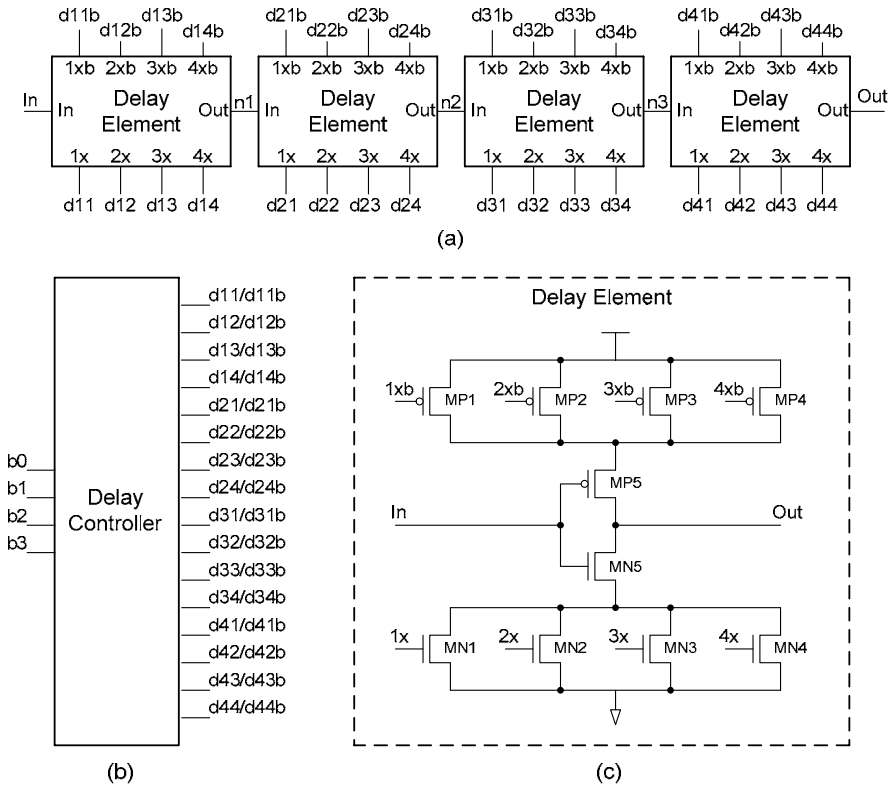

Fig. 2. Circuit diagram of 4-bit digitized delay block. (a) Delay element chain, (b) delay controller, (c) Delay element

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2.2 Quarter phase detector

Fig. 3 (a) and Fig. 3 (b) shows the quarter-phase detector block and its timing diagram operating as a key role in this system. Initially, all transistors are in an ON state during the reset period to maintain the same voltage level between the operating node, V1, and the reference node, V2. During the reset clock period, the MN0, MN2, MP2 transistors are in OFF states to maintain the reference voltage. During the V1-increase period, MP1 is ON and MN1 is OFF so that the capacitor, C1, can be in a charge state. On the other hand, MP1 is OFF and MN1 is ON so that capacitor, C1, can be in a discharge state during the V1-decrease period. The V1 and V2 nodes are connected to the input ports of the comparator block to amplify the voltage difference and produce the control values, logic one for an up signal or zero for a down signal.

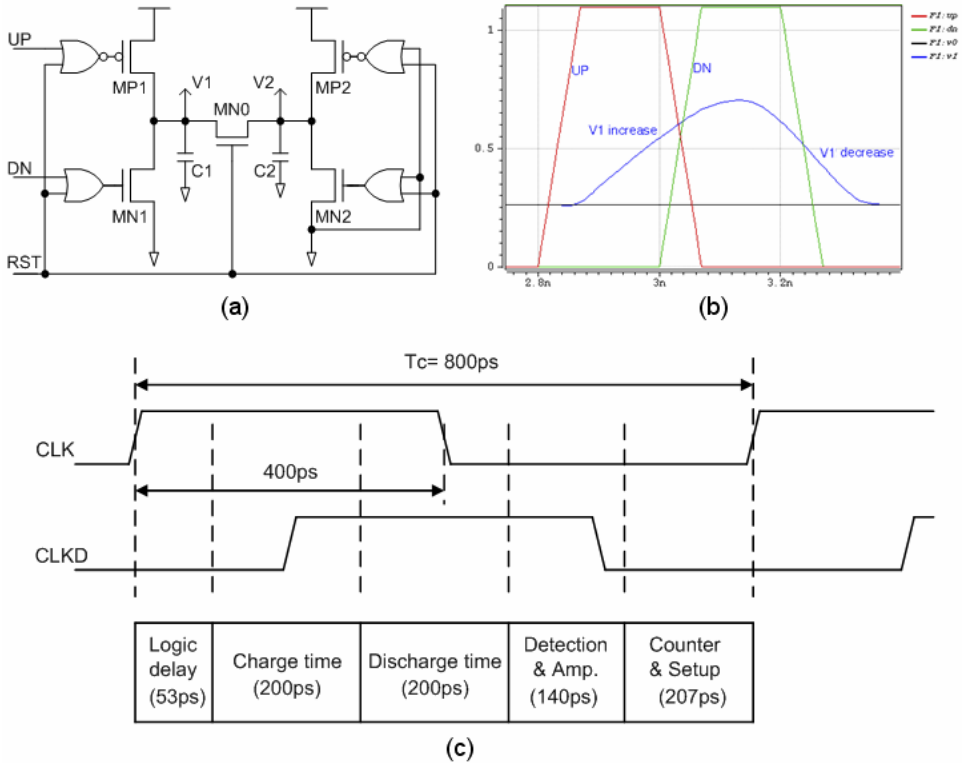

Fig. 3. Circuit & timing diagram of quarter phase detector and measurement results for timing critical path. (a) Circuit diagram of quarter phase detector, (b) Timing operation waveform of quarter phase detector, (c) Measurement results for timing critical path

2.3 Up-Down counter

A four-bit counter calculates the binary weight according to the logic value of the input signal. The range of the delay value of the digitized delay is from 0000 to 1111, so the number of delay step is from zero to fifteen. A

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delay step can be moved up and down by one step. This adjustment of step is continuously performed to reach the target delay amount in every clock cycle. The highest state is 1111 and the lowest state is 0000 in binary system. When the counter is in a 1111 state, even though the up signal arrives, the counter keeps the 1111 value since it is the highest state. A similar mechanism is operated in the lowest state. One of the advantages of this system is that additional signals are not needed such as reset or up-down signals that are typically used in general clock frequency doubling system. The proposed structure eliminates the offset voltage by means of creating a reset signal in every cycle.

3 Measurement results

The implementation has been evaluated using Samsung 0.13-micron CMOS process technology. The measurement results provide a critical path delay of the designed clock frequency doubler at 800 ps, and the detailed time delay of each component is shown in Fig. 3 (c). The delay of logic, 53 ps, is needed to produce UP/DN signals from the CLK and CLKD that are generated by the digitized delay block. Therefore, the charge and discharge time periods are slightly retarded through the logic. Two 200 ps time periods are spent to do charge and discharge operations. As shown in the Fig. 3 (c), the 140 ps time intervals were used to detect the time difference and amplify it to logic values using a quarter phase detector and a comparator circuit that has been made up of sense amplifier. Finally, the delays of the 4 bit counter and the setup time have spent the cycle time of 207 ps. Because the overall critical path delay has been measured at 800 ps, this system can operate fast enough to produce 2.5 GHz by utilizing this simple circuit configuration.

4 Conclusion

We have presented the design and measurement results of fully digital automatic adjustable clock frequency doubler without feedback loops. The duty cycle amount is automatically adjustable using a digitized delay block and a counter so that we can achieve a robust and stable design. This design method simplifies the design structure and allows the circuits to operate over a wider range of input frequency variation as well as support a higher frequency range. The measurement results provide the operation range from 650 MHz to 2.5 GHz. This fully digital clock frequency doubler can be used for wide digital applications requiring very high speeds, robustness, and time on demand requirement units.

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