ELectronics EXpress

IEICE Electronics Express, Vol.7, No.9, 621–627

DSP-based flexible digital hysteresis in switched capacitor active power filter

Nasrudin Abd. Rahim[1a)] **and Mohd Amran Mohd Radzi**[2b)]

[1] *Center of Research for Power Electronics, Drives, Automation and Control University of Malaya, 50603 Kuala Lumpur, Malaysia*

[2] *Department of Electrical and Electronic Engineering Universiti Putra Malaysia, 43400 UPM Serdang, Selangor, Malaysia*

a) *nasrudin@um.edu.my*

b) *amranmr@eng.upm.edu.my*

Abstract: This paper proposes implementation of digital signal processor (DSP) to perform flexible-band digital hysteresis current control in a switched capacitor active power filter (SCAPF). By integrating hysteresis current control with digital-based neural network harmonic detection, the proposed SCAPF forces the supply current to be sinusoidal, to have low current harmonics, and to be in phase with the line voltage. Simulation on MATLAB Simulink verified the controller's algorithm design, and a purpose-built laboratory SCAPF system tested its feasibility.

Keywords: DSP, hysteresis, switched capacitor active power filter

Classification: Science and engineering for electronics

References

[1] M. El-Habrouk and M. K. Darwish, "A new control technique for active power filters using a combined genetic algorithm/conventional analysis," *IEEE Trans. Ind. Electron.*, vol. 49, no. 1, pp. 58–66, Feb. 2002.

[2] T. Kandil, L. Lopes, and W. Xu, "Analysis and design of a new current controlled switched capacitor filter for harmonic mitigation," *Electric Power Comp. Syst.*, vol. 33, pp. 1–20, 2005.

[3] M. A. M. Radzi and N. A. Rahim, "Neural network and bandless hysteresis approach to control switched capacitor active power filter for reduction of harmonics," *IEEE Trans. Ind. Electron.*, vol. 56, no. 5, pp. 1477–1484, May 2009.

[4] W. Shireen and L. Tao "A DSP-based active power filter for low voltage distribution systems," *Electric Power Systems Research*, vol. 78, no. 9, pp. 1561–1567, Sept. 2008.

[5] X. Lin-Shi, F. Morel, J.-M. Rétif, and B. Allard, "A New Direct Current Control for a Permanent Magnet Synchronous Machine," *Electric Power Comp. Syst.*, vol. 36, no. 9, pp. 897–913, Sept. 2008.

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

IEICE Electronics Express, Vol.7, No.9, 621–627

1 Introduction

Power quality of ac supply is a major issue discussed recently. Power electronics devices and applications in electricity supply networks increase nonlinear loads and produce nonsinusoidal current, causing harmonic distortion and low power factor. Compensation of the generated harmonics and correction of the line power factor are necessary. Switched capacitor active power filter (SCAPF) is introduced as an alternative to inverter-based active power filter (APF) [1]. It brings a new dimension through reduced components and ratings (especially ac capacitors), operated at low switching frequency, and implemented with less complicated control circuit (no need to regulate the dc voltage bus) [2].

Fig. 1 shows the proposed configuration for this work. Two ac capacitors (C_1 and C_2) are connected in series with two main bidirectional switches (S_1 and S_2) connected parallel to the ac line. S_1 and S_2 work in antiphase so that the filter current flows through the branches alternately. However, in the experiment setup, since both switches operate with a small deadband during their transition period, a small resistor R with another bidirectional switch S_3 is required, to allow smooth transfer of current between both capacitor branches at that period. Both capacitors are charged, and switching patterns generated, through a hysteresis algorithm. The filter current's rate of change is controlled by a limiting inductor. The two capacitor branches made the circuit's operation more flexible, allowing switching to occur at any instant and also at any switching frequency. All switches are connected to the digital signal processor (DSP), which performs full digital control algorithm. Two current sensors that measure load and filter currents are connected to the DSP. A voltage sensor to measure voltage at point common coupling is also

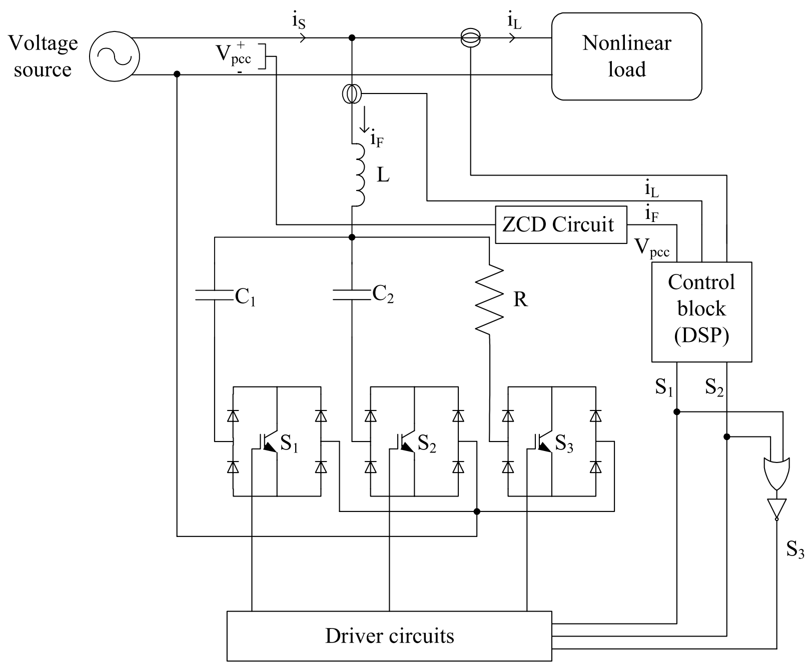

Fig. 1. Configuration of SCAPF.

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

IEICE Electronics Express, Vol.7, No.9, 621–627

connected for zero crossing detection (ZCD).

2 Implementation of digital signal processor

The new proposed digital hysteresis control strategy, flexible-band approach, combines advantages of bandless approach [3] and standard fixed band approach. Its help the SCAPF to operate in a more stable switching frequency as it is flexible to hysteresis's band selection. Besides that, a harmonic detection technique by using modified artificial neural network (ANN) is used with suitable learning rate attached to it. Design and development process of both control techniques considers DSP capability as a small-scale process controller, to miniaturize systems and for high-speed performance. Previous works [4, 5] report the importance of DSP in implementing, and in testing by experiment, the designed algorithms, in ensuring expected performance.

Fig. 2 (a) shows a proposed structure of control system developed in the DSP. The measurement processed by the DSP starts from the ZCD circuit's signal detection. The ZCD's input module program initializes the starting time of the DSP's sampling operation. Measurement of load current i_L and filter current i_F are processed by an analogue-to-digital (ADC) module in the DSP, analogue values converted to digital ones. i_L is processed by the harmonic detection algorithm, ANN, for harmonic current i_H. This current is compared with i_F in the hysteresis algorithm, to produce pulse signals equivalent to those of S_1 and S_2. Same sampling frequency is applied to all modules and parts in the control system. A TMS320F2812 DSP implements the control algorithms explained in the next section. The programming part are developed and written in C language and then compiled in Code Composer Studio.

3 Control techniques

Fig. 2 (a) also shows flexible-band module for the proposed hysteresis algorithm. Two main parts are designed: switching frequency detection and band selection. The switching frequency detection part determines the updated operating switching frequency produced by the hysteresis algorithm. The band selection part selects whether to use bandless, or band, approach, in the hysteresis algorithm.

Fig. 2 (b) shows an operational flexible-band digital hysteresis control in both bandless and band approaches. Initially, bandwidth ΔI, high-level frequency limit f_H, and low-level frequency limit f_L need to be configured. The switching frequency detection algorithm captures the switching period and calculates the switching frequency f_S. Then, the band selection algorithm checks the condition for band. If the hysteresis operation is bandless, then the algorithm checks whether the f_S is higher than f_H or if it is not. If it is higher, then the band selection algorithm changes the hysteresis operation to band approach; else, no change to band selection. On the other hand, if the hysteresis operation is with band then the selection band algorithm

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

IEICE Electronics Express, Vol.7, No.9, 621–627

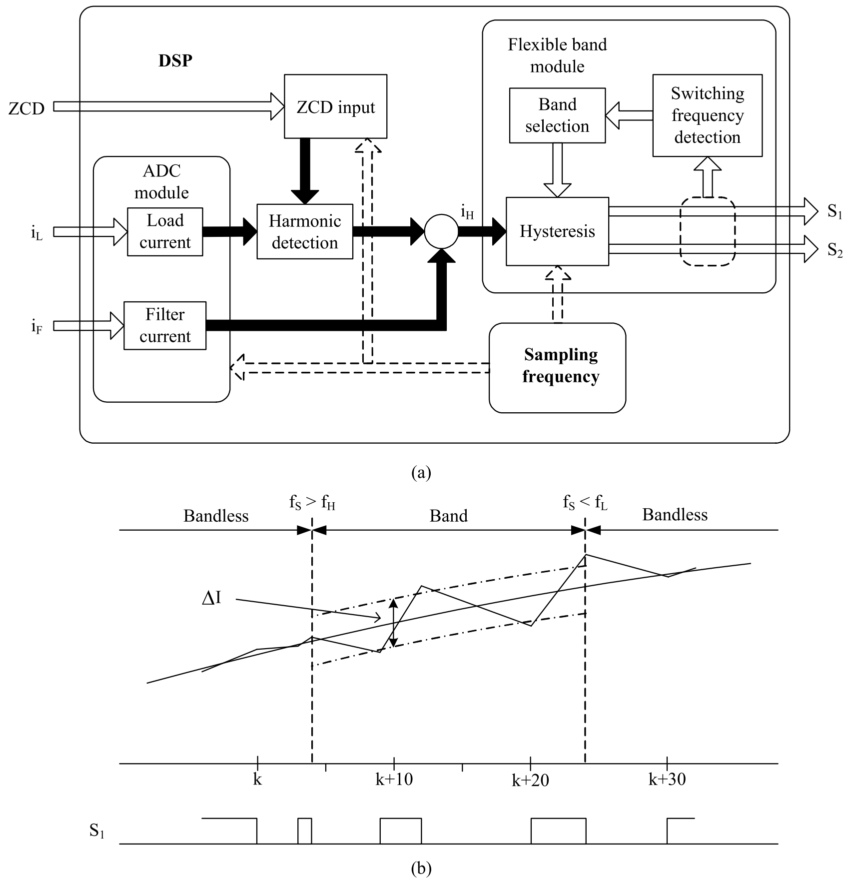

Fig. 2. (a) Control system in DSP. (b) Flexible-band digital hysteresis.

checks whether f_S is lower than f_L or if it is not. If it is lower, the hysteresis operation is changed to bandless, else, no change.

This proposed algorithm solves possible problems such as high ripple in filter current due to switch changes state at the desired sample rather than at the bandwidth limit in fixed-band mode, and losses due to high switching frequency in bandless approach.

In the ANN algorithm for harmonic detection technique, for each sample k in digital operation with sampling time Δt and fundamental frequency ω, the nonlinear load current i_L is represented by a fundamental component and a harmonic component as shown:

$$\begin{aligned} i_L(k) &= \sum_{n=1,2,3,\ldots}^{N} \left[w_{1n} \sin\left(nk\omega\Delta t\right) + w_{2n} \cos\left(nk\omega\Delta t\right)\right] \\ &= w_{11} \sin(k\omega\Delta t) + w_{21} \cos(k\omega\Delta t) \\ &\quad + \sum_{n=2,3,\ldots}^{N} \left[w_{1n} \sin\left(nk\omega\Delta t\right) + w_{2n} \cos\left(nk\omega\Delta t\right)\right] \end{aligned} \tag{1}$$

where w_{1n} and w_{2n} are the amplitudes of the sine and cosine parts of the measured nonlinear load current, an n is the number of harmonics, to N maximum number. Both terms can be represented in vector form

$$\bar{i}_L(k) = \overline{W}^T \overline{X}(k) \tag{2}$$

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

IEICE Electronics Express, Vol.7, No.9, 621–627

where the weight matrix $\overline{W}^T = [w_{11}w_{21} \dots w_{1N}w_{2N}]$ and the sine and cosine vector

$$\overline{X}(k) = \begin{bmatrix} \sin(k\omega\Delta t) \\ \cos(k\omega\Delta t) \\ \vdots \\ \sin(Nk\omega\Delta t) \\ \cos(Nk\omega\Delta t) \end{bmatrix}$$

The ANN algorithm is used to train $\overline{W}^T$ to generate the right value of $i_L(k)$. The Widrow-Hoff (W-H) weights updating algorithm is used to minimize the average square error $e(k)$ between the actual measured signal $i_L(k)$ and the estimated signal $i_{est}(k)$, which can be written as:

$$\overline{W}(k+1) = \overline{W}(k) + \frac{e(k)\overline{X}(k)}{\overline{X}^T(k)\overline{X}(k)} \tag{3}$$

where $e(k) = i_L(k) - i_{est}(k)$ and $\overline{X}^T(k)\overline{X}(k)$ is the square of the norm of $\overline{X}(k)$. However, the dimension of the weight matrix is updated according to N, which lengthens calculation time, relatively. A simplified algorithm proposes that

$$\overline{W}(k+1) = \overline{W}(k) + \frac{\alpha e(k)\overline{Y}(k)}{\overline{Y}^T(k)\overline{Y}(k)} \tag{4}$$

where $\overline{W}^T = [w_{11}w_{21}]$, $\overline{Y} = \begin{bmatrix} \sin(k\omega\Delta t) \\ \cos(k\omega\Delta t) \end{bmatrix}$ and α is the learning rate.

This modified W-H algorithm needs only to update the two weights of the fundamental component, making it independent of the number of harmonic orders present. The suitable learning rate is determined by considering how fast and good the algorithm could produce i_H and minimize THD of i_S. The i_H can be produced from load current deduction (from load current's fundamental sine part).

4 Simulation and experimental results

The circuit was developed and tested on a powerful MATLAB Simulink together with SimPowerSystems block. The laboratory prototype was also developed for experimental testing. A nonlinear load was developed by using a diode bridge rectifier, feeding an inductive load comprising an 80-mH inductor and a 17-Ω resistor. Sampling time was set as 40 μs (25-kHz sampling frequency). The voltage supply is 100 V_{rms}. Two insulated-gate bipolar transistors (IGBT) and twelve fast recovery diodes were used to develop bidirectional switches, connected to 120-μF capacitors. An additional bidirectional switches connected to a 15-Ω resistor was developed in the experimental setup. The learning rate is set to 0.003. The ΔI was set to 0.7 A, which was about 5% of peak-to-peak expected operating current. f_H was set to 4.167 kHz (inverse of multiplication of six to sampling time) and the f_L was set to 2 kHz (inverse of multiplication of ten to sampling time).

Fig. 3 shows simulated and experimental waveforms and THDs of source current i_S without SCAPF connection (Fig. 3 (a) and Fig. 3 (b)), and later

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

by connecting the SCAPF (Fig. 3 (c) and Fig. 3 (d)). Fig. 3 (c) and Fig. 3 (d) also show each capacitor voltage, proving that the SCAPF still can operate without regulating them. Then, Fig. 3 (e) and Fig. 3 (f) presents waveforms of switching patterns from one of the bidirectional switches connected to the capacitor. The results show the flexible-band approach was able to operate the SCAPF to compensate harmonic current. The power factor in experimental testing increased from 0.87 to 0.98. The switching patterns showed stable performance. Quantitative analysis on ripple's percentage and power losses was also carried out not only to this proposed approach, but also to fixed band and bandless for purpose of comparison. This approach recorded ripple between 5 to 13%, as compared to bandless (3 to 11%), and fixed band (7 to 17%). Through this approach too, the SCAPF produced output power of 218 W, resulting losses of 12 W or 5.2% from input of SCAPF (230 W), as compared to bandless (203 W and losses of 27 W or 11.7%), and fixed band (223 W and losses of 7 W or 3%). It performs most stable as ripple closes to bandless and power losses closes to fixed band. The highest ripple was recorded in fixed band and the highest losses were in bandless.

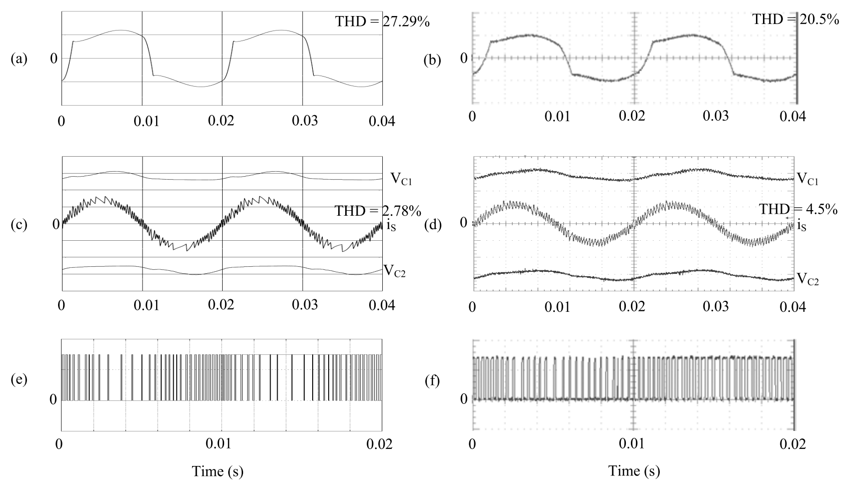

Fig. 3. (a) Source current (simulation) without connection in 5 A/div. (b) Source current (experiment) without connection in 5 A/div. (c) Source current and capacitor voltage (simulation) after connection in 5 A/div and 50 V/div. (d) Source current and capacitor voltage (experiment) after connection in 5 A/div and 50 V/div. (e) Switching pattern (simulation) in 10 V/div. (f) Switching pattern (experiment) in 10 V/div.

5 Conclusion

The proposed digital control algorithms, flexible-band hysteresis current control, together with modified ANN algorithm, were successfully implemented to the SCAPF. The flexible-band digital hysteresis was implemented to produce a stable switching pattern. The modified ANN was developed with a

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010

suitable learning rate to detect harmonic component. The DSP was successfully programmed and run to operate the SCAPF in the experiment. The SCAPF successfully compensated harmonic current, reduced the THD value, and increased the power factor to near unity.

DOI: 10.1587/elex.7.621
Received March 01, 2010
Accepted April 02, 2010
Published May 10, 2010