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A CMOS high-speed pulse swallow frequency divider for ΔΣ fractional-N PLL's

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Abstract: A high-speed pulse-swallow frequency divider suitable for ΔΣ fractional-N synthesizers is proposed. The proposed structure employs the retiming scheme for the modulus control signal to extend the timing margin, thus remarkably increasing the maximum operating speed. Moreover, unlike the conventional structure, the modulus control signal is set and reset by a single triggering signal to eliminate the unwanted offset at the total division ratio. It simplifies the interface logic between the divider and the ΔΣ modulator in ΔΣ fractional-N PLL's. Simulation results show that the proposed divider provides over three times faster operating speed than the conventional one. The proposed divider has been successfully verified in CMOS RF ΔΣ fractional-N frequency synthesizers.

Keywords: pulse swallow counter, frequency divider, fractional-N PLL

Classification: Integrated circuits

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1 Introduction

A programmable frequency divider in PLL frequency synthesizers divides the voltage-controlled oscillator (VCO) output frequency down to around a wanted reference frequency. It requires high-speed operation as well as flexible and stable control of division ratio. The most conventional structure of the programmable frequency divider in PLL is a pulse-swallow type based on a dual-modulus prescaler (DMP), as shown in Fig. 1 (a). It comprises a DMP (P/P + 1), a programmable counter (A), and a swallow counter (B) [1, 2]. The fundamental speed limitation of this structure usually comes from the critical delay path of the modulus control (MC) signal. When the MC delay is longer than the DMP output period, the total division ratio becomes wrong and the PLL go to a failure. A pipelined retiming of the MC signal was proposed to effectively resolve the MC delay problem [3]. Also, employing a timing window generation by using a finite-width pulse generator was also shown to be effective [4]. Nevertheless, it is found that those previous structures inherently possess an unwanted division ratio offset of one. It makes the interface logic between the $\Delta\Sigma$ modulator and the pulse-swallow divider complicated in $\Delta\Sigma$ fractional-N PLL's.

In this work, a new structure of a pulse-swallow frequency divider is proposed. It is basically based on the retiming structure to alleviate the MC delay problem like in [3], and the undesired division ratio offset is avoided by a new structural design. In addition, another timing issue that is critical but not often recognized in the literature is also addressed.

2 Circuit design and results

2.1 Conventional architecture

The conventional pulse swallow divider [1, 2] is shown in Fig. 1 (a), and its timing diagram is shown in Fig. 1 (b). After B counter completes its counting, B_{out} sets MC via SR latch (transition①), leading to the DMP division ratio change from P + 1 to P. The MC state changes after the MC delay τ_{MC}, for which the delay path is drawn by the dotted line in Fig. 1 (a). If τ_{MC} becomes too large, the MC signal would not be able to switch the DMP modulus correctly in a given timing margin, leading to a wrong division ratio. Thus, τ_{MC} limits the maximum operating speed. Reducing τ_{MC} is one of the critical design issues in this type of divider.

Another design issue is the unwanted division ratio offset. After A counter completes its counting, A_{out} resets MC (transition②). Note that the division ratio for the first half period is $(B+1)\times(P+1)$ rather than $B\times(P+1)$. It is because MC is instantly reset by A_{out} whereas B_{out} is reset at the next rising edge of P_{out} after MC becomes zero. Thus, considering that the division ratio of the next half period is $(A - B - 1)\times P$, the total division ratio N is given by $PA + B + 1$. It indicates that the total division ratio has an offset of one greater than the original setting value. Due to this offset, the "B + 1" part of the total division ratio N can never be set to zero. It makes the total division ratio setting complicated when it is used for $\Delta\Sigma$ fractional-N

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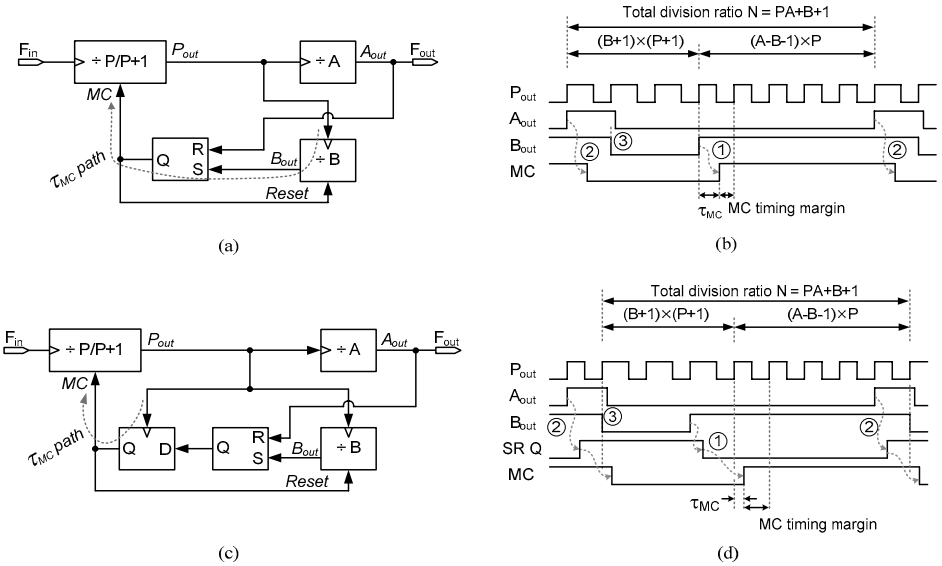

Fig. 1. (a) Conventional pulse-swallow divider. (b) Timing diagram of structure (a). (c) Conventional pulse-swallow divider with MC retiming. (d) Timing diagram of structure (c).

PLL's. In ΔΣ fractional-N PLL's, the ΔΣ modulator output is supposed to be added to N. Thus, the case of "B+1+ΔΣ modulator output" = "0" must be avoided, which means the total division ratio setting should be mapped to some other different settings by readjusting "A" value in order to avoid the case of "B + 1 + ΔΣ modulator output" = "0". Such complicated logic can be greatly simplified if the division ratio offset does not exist. If so, a simple addition of B counter and ΔΣ modulator output would be sufficient for the interface logic.

Another potential problem of the structure is the possible malfunction of the SR latch depending on the relative timing of the falling edges of A_{out} and B_{out}. As shown by the transition③ in Fig. 1 (b), the falling edge of A_{out} must arrive later than B_{out}. Otherwise, MC would accidentally change to make a wrong division ratio.

The MC timing margin issue of the conventional structure can be mitigated by employing a pipeline scheme at the MC signal transfer path. Fig. 1 (c) shows the structure proposed in [3] that uses a D flip-flop to retime the MC. Due to the retiming of MC, the MC delay path is greatly reduced and thus the MC timing margin is extended, as illustrated by the transition① in Fig. 1 (d). Nevertheless, the other two issues mentioned above (the unwanted division ratio offset and the possible malfunction of SR latch) still exist in this structure.

2.2 Proposed architecture

We propose a new structure of pulse swallow frequency divider. The proposed structure is shown in Fig. 2 (a). It adopts the MC retiming scheme by using a D flip-flop. Thus, the MC delay τ_{MC} of this structure is much smaller

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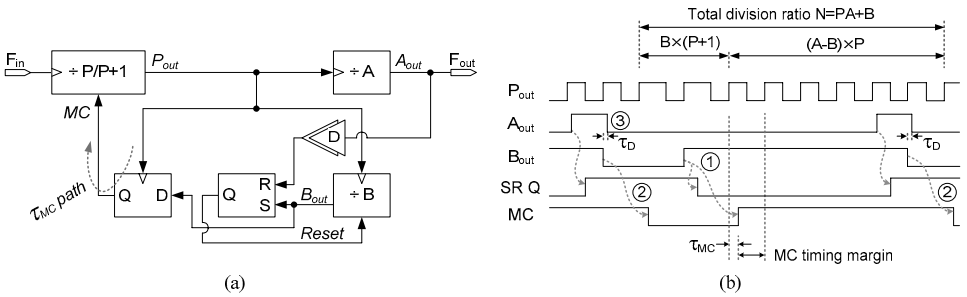

Fig. 2. (a) Proposed pulse-swallow frequency divider. (b) Timing diagram.

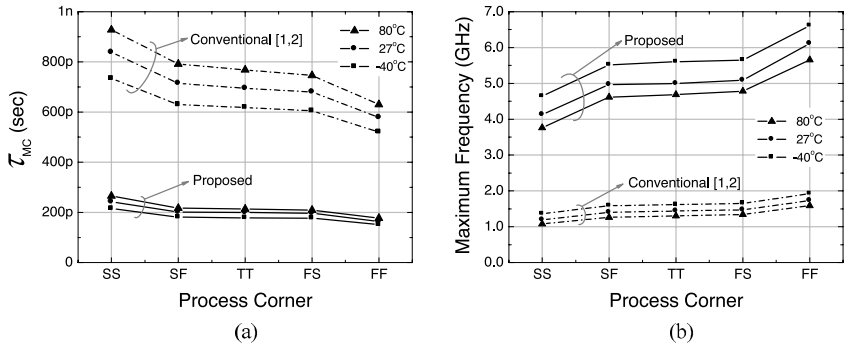

Fig. 3. Simulation results of the proposed pulse-swallow divider over process and temperature corners. (a) MC delay (τ_{MC}). (b) Maximum operating speed.

than the conventional one in Fig. 1 (a) [1, 2] and comparable to the previous retiming structure in Fig. 1 (c) [3]. As illustrated in Fig. 2 (b), the larger MC timing margin guarantees higher operating speed.

In the conventional structures, the MC signal's set and reset are triggered by different signals, that is, set by B_{out} and reset by A_{out} as illustrated by the transition① and ②, respectively, in Fig. 1 (b) and (d). It was the root cause of the unwanted division ratio offset of one. However, in the proposed structure, the MC signal's set and reset are triggered by a single signal, that is B_{out}. As a result, the division ratio of the first half period is given by $B \times (P + 1)$ and the next half period has a division ratio of $(A - B) \times P$. Thus, the total division ratio is simply given by $PA + B$. Such no-offset structure greatly simplifies the $\Delta\Sigma$ modulator interface logic when it is used in $\Delta\Sigma$ fractional-N PLL's. Another design improvement of this structure is that the delay element D is inserted between A counter and SR latch. This ensures that A_{out} falling edges always arrive later than the B_{out} falling edge, as illustrated in the transition③ in Fig. 2 (b).

The proposed divider of Fig. 2 is designed in 0.18 μm CMOS technology. Fig. 3 shows the simulation results of τ_{MC} and the maximum operating frequency under various conditions including the process corners of slow/typical/fast and temperature variation of $-40/27/80$°C. As can be seen, τ_{MC} is reduced by 71.2% compared to the conventional structure of Fig. 1 (a).

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Therefore, the maximum operating frequency is increased approximately by three times. The unwanted division ratio offset and the malfunction of the SR latch are not observed in the simulations either. The proposed pulse swallow divider has been verified by embedding it to GHz $\Delta\Sigma$ fractional-N frequency synthesizers fabricated in 0.18 μm CMOS [5] and also in 0.13 μm CMOS [6].

3 Conclusion

A high-speed pulse swallow frequency divider suitable for $\Delta\Sigma$ fractional-N synthesizers is presented. The MC retiming scheme greatly extends the timing margin, thus providing much higher operating speed. Unlike the conventional structures, the single-signal triggering of the MC signal eliminates the unwanted offset at the total division ratio, which greatly simplifies the interface logic in $\Delta\Sigma$ fractional-N PLL's. Simulation results show that the proposed divider structure provides about three times faster operating speed than the conventional one. The proposed divider is also successfully verified in GHz CMOS $\Delta\Sigma$ fractional-N frequency synthesizers.

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