ELectronics EXpress

IEICE Electronics Express, Vol.8, No.1, 1–7

A three-phase five-level inverter for DTC drives application

Nasrudin Abd Rahim[a)], **Mohamad Fathi Mohamad Elias, and Hew Wooi Ping**

Centre of Research for Power Electronics, Drives, Automation & Control (UMPEDAC), Faculty of Engineering, University of Malaya

50603 Kuala Lumpur, Malaysia

a) *nasrudin@um.edu.my*

Abstract: This paper presents a new three-phase five-level inverter for direct torque control (DTC) drives application. The advantages of the inverter are reduced output harmonics, switching losses and number of power switches. The multilevel PWM modulation method as well as output voltage analysis based on symmetrical sampling are presented. The proposed inverter is compared with the conventional inverter in terms of its current's total harmonics distortion (THD). Experimental results of DTC drive of permanent magnet synchronous motor (PMSM) are also presented for verification of its proposed function.

Keywords: Direct torque control, PMSM drives, multilevel inverter

Classification: Science and engineering for electronics

References

[1] L. Zhong, M. F. Rahman, W. Y. Hu, K. W. Lim, and M. A. Rahman, "A direct torque controller for permanent magnet synchronous motor drives," *IEEE Trans. Energy Convers.*, vol. 14, pp. 637–642, 1999.

[2] T. Lixin, Z. Limin, M. F. Rahman, and Y. Hu, "A novel direct torque controlled interior permanent magnet synchronous machine drive with low ripple in flux and torque and fixed switching frequency," *IEEE Trans. Power Electron.*, vol. 19, pp. 346–354, 2004.

[3] N. A. Rahim, K. Chaniago, and J. Selvaraj, "A Modified H-bridge Multilevel Inverter for Photovoltaic System," *IEICE Electron. Express*, vol. 7, no. 11, pp. 751–758, 2010.

[4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2553–2580, 2010.

[5] P. Sung-Jun, K. Feel-Soon, L. M. Hyung, and U. K. Cheul, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, vol. 18, pp. 831–843, 2003.

[6] V. G. Agelidis, D. M. Baker, W. B. Lawrance, and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications," *Proc. IEEE Int. Symp. Ind. Electron. 1997, ISIE '97*, vol. 2, pp. 589–594, 1997.

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

[7] N. A. Rahim, J. Selvaraj, and K. Chaniago, "A Novel PWM Multilevel Inverter for PV Application," *IEICE Electron. Express*, vol. 6, no. 15, pp. 1105–1111, Aug. 2009.
[8] F. Wanmin, R. Xinbo, and W. Bin, "A Generalized Formulation of Quarter-Wave Symmetry SHE-PWM Problems for Multilevel Inverters," *IEEE Trans. Power Electron.*, vol. 24, pp. 1758–1766, 2009.
[9] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, pp. 518–523, 1981.
[10] M. F. Rahman, M. E. Haque, T. Lixin, and Z. Limin, "Problems associated with the direct torque control of an interior permanent-magnet synchronous motor drive and their remedies," *IEEE Trans. Ind. Electron.*, vol. 51, pp. 799–809, 2004.

1 Introduction

In variable speed drives application today, DTC has emerged as the best and most promising solution to achieve high dynamic drive performance. However, with the conventional three-level inverter and hysteresis approach, the torque and flux ripples as well as the current harmonics are still high and therefore requiring output filter [1]. One solution is to use pulse-width modulation (PWM) or space vector modulation (SVM). Another solution is to use multilevel inverter, as more voltage vectors are available for selection enable lower voltage switching or *dv/dt's* [2]. Besides motor drives, multilevel inverters have found many successful industrial applications ranging from medium to high power levels such as in power conditioning devices, power distribution and generation [3, 4]. This paper presents a new configuration of multilevel inverter for DTC-based motor drives.

2 The proposed multilevel inverter topology

The proposed inverter in Fig. 1 is developed from the five-level H-bridge topology [5] where one arm of the H-bridge is connected to the motor terminal and the other to the neural point N. This topology has an additional bidirectional power switch connected between the first arm and the midpoint of the capacitor, allowing the inverter to produce five output levels ($-v_{dc}$, $-v_{dc}/2$, 0, $v_{dc}/2$, v_{dc}). There are 3 types of bidirectional power switches, in which one of them is shown in Fig. 1. The other two comprise both 2 IGBTs with diodes, one has common emitter-emitter configuration [4] and the other has common emitter-collector configuration [6]. But, their use would increase control complexity as they require two gate drives. In comparison with other five-level topologies such as cascaded H-bridge (CHB) and neutral point clamped (NPC)/H-bridge, the proposed topology has relatively less three power switches per phase [4]. Connection to the capacitor midpoint may unbalance the capacitor's voltage. Here, the capacitor's voltage is fixed with two rectifiers, one rectifier for each capacitor. For better regulation of dc-link voltage and to cancel lower order input current harmonics, use of a multi-pulse rectifier and phase shifting transformer is recommended.

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

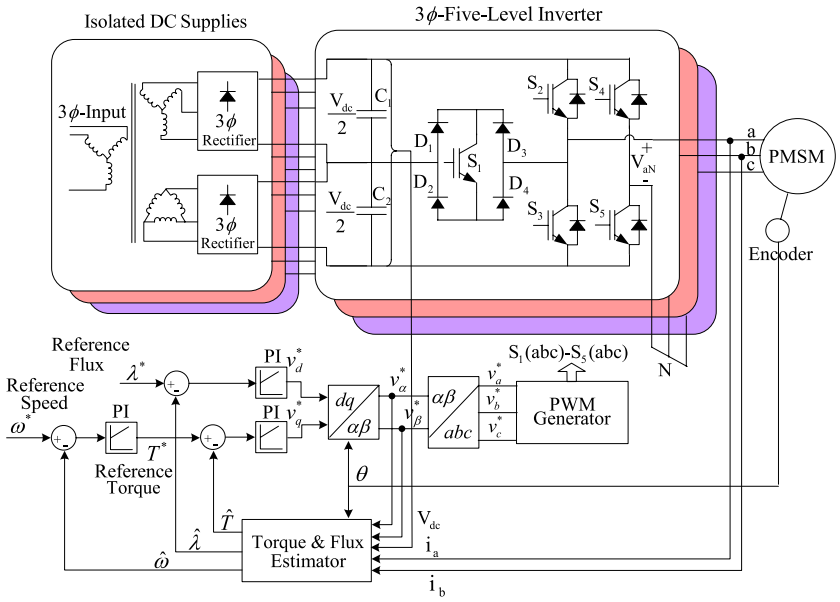

Fig. 1. The proposed three-phase multilevel inverter.

3 Multilevel PWM modulation and output voltage analysis

Modulation index, m_a of the proposed multilevel inverter is defined as

$$m_a = V_{ref}/2V_c \tag{1}$$

where V_{ref} is the amplitude of the reference voltage and V_c is the amplitude of the carrier signal. The PWM signal is generated by comparing one symmetrical triangular carrier with two voltage references [7]. Here, symmetrical sampling based PWM modulation is implemented. Fig. 2 (a) shows PWM signal generation of Phase A. The switching patterns for all switches are represented by logical operators, Eq. (2) – (6). From these equations, it is noted that S4 and S5 operate at fundamental frequency whereby the rest of switches operate very close to the switching frequency. The truth table for the inverter is given by Table I. The PWM signals for Phase B and C are also generated using the same technique, with their references are shifted by 120^0 and 240^0 respectively.

$$S_1 = S_{V_{ref1}} \cdot M_1 + \bar{S}_{V_{ref2}} \cdot M_2 + S_{V_{ref1}} \cdot M_3 + \bar{S}_{V_{ref2}} \cdot M_4 \tag{2}$$

$$S_2 = S_{V_{ref2}} \cdot M_2 + \bar{S}_{V_{ref1}} \cdot M_3 \tag{3}$$

$$S_3 = \bar{S}_{V_{ref1}} \cdot M_1 + S_{V_{ref2}} \cdot M_4 \tag{4}$$

Table I. Truth table of inverter output phase voltage.

S_1	S_2	S_3	S_4	S_5	V_{out}
0	1	0	0	1	V_{dc}
1	0	0	0	1	$V_{dc}/2$
0	0 or 1	1 or 0	0 or 1	1 or 0	0
1	0	0	1	0	$-V_{dc}/2$
0	0	1	1	0	$-V_{dc}$

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

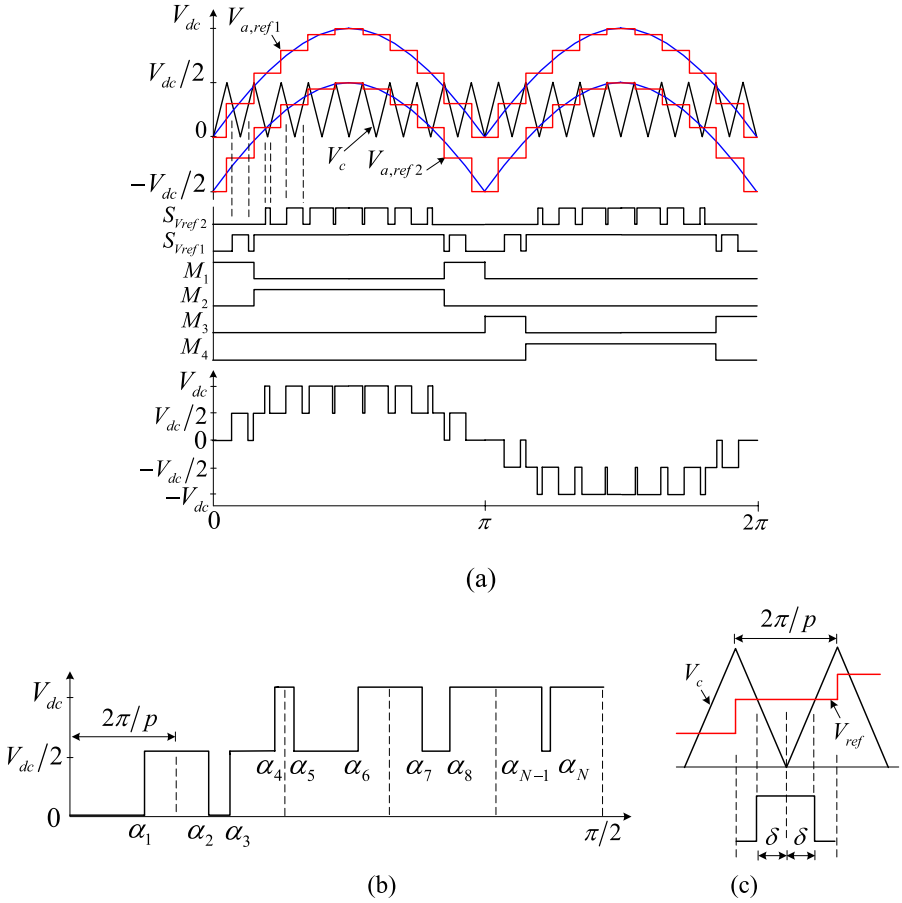

Fig. 2. (a) PWM signal generation of Phase A. (b) Quarter-wave symmetrical output (c) Pulse generation.

$$S_4 = M_3 + M_4 \tag{5}$$

$$S_5 = M_1 + M_2 \tag{6}$$

The inverter's output phase voltage can be represented using Fourier series expansion as

$$V(\omega t) = \sum_{n=1}^{\infty} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{7}$$

In case of the output voltage is quarter-wave symmetrical and odd function characteristics as in Fig. 2 (b), Eq. (7) can be reduced to

$$V(\omega t) = \sum_{n=1}^{\infty} b_n \sin(n\omega t) \tag{8}$$

where, b_n can be represented as below for N (odd or even) number of switching angles, α_i per quarter period [8].

$$b_n = \begin{cases} 0, & n = \text{even} \\ \dfrac{2V_{dc}}{n\pi} \displaystyle\sum_{i=1}^{N} \rho_i \cos n\alpha_i & n = \text{odd} \end{cases} \tag{9}$$

where ρ_i is

$$\rho_i = \begin{cases} 1, & \alpha_i \text{ for rising edge} \\ -1, & \alpha_i \text{ for falling edge} \end{cases} \tag{10}$$

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

Fig. 2 (c) shows a pulse generation where the pulse's width is equal to 2δ as a result of symmetrical sampled modulation. The carrier's period is defined as $2\pi/p$ where p is the frequency modulation ratio given by $p = f_s/f_1$. f_s is the carrier frequency and f_1 is the fundamental frequency.

4 Principles of DTC drives

Since its first introduction by Takahashi in 1986 [9], many researches on DTC drives have been carried out mainly to improve its control algorithm, solving several related issues and implementation in various inverters. In fact, nowadays DTC has becomes the state-of-the-art in motor control. Its advantages are faster torque response compared with that of PWM current control and less dependence on parameters, in which depending only on the stator resistance. It is also inherently sensorless where encoder is not required to run the motor as long as the initial rotor position is known. DTC drives employing PMSM can increase up to 30% more energy efficiency than the conventional induction motor, providing the best solution to industrial motor drives. The basic idea of DTC is to select the appropriate voltage vector based on the difference between the reference and the estimated torque and flux linkage. Fig. 1 shows the scheme implemented, selected from several DTC control schemes. The scheme uses three PI controllers for controlling the speed, torque and flux. The stator flux, λ and developed torque, T of the motor are estimated by the following equations

$$\lambda_\alpha = \int (v_\alpha - Ri_\alpha)dt \tag{11}$$

$$\lambda_\beta = \int (v_\beta - Ri_\beta)dt \tag{12}$$

$$|\lambda| = \sqrt{\lambda_\alpha^2 + \lambda_\beta^2} \angle \tan^{-1}\left(\frac{\lambda_\beta}{\lambda_\alpha}\right) \tag{13}$$

$$T = \frac{3P}{2}(\lambda_\alpha i_\beta - \lambda_\beta i_\alpha) \tag{14}$$

where v_α, v_β and i_α, i_β are the stator voltages and currents in the stationary reference frame ($\alpha\beta$). R is the stator resistance and P is the number of pole pairs. The reference torque is generated based on the difference between the reference and the actual speed of the motor via PI controller whereas the reference flux is set to the nominal motor flux linkage. These two references are compared with the estimated stator flux and torque obtained using Eq. (13) and Eq. (14), and the errors are fed to two other PI controllers. Outputs of the controllers are reference voltages in rotor reference frame (dq) and converted into stator reference frame (abc) using rotor angle, θ for PWM signal generation. Implementation of DTC drives involves several issues. For instance, any dc offset occurs in the sensed stator currents will cause error in the stator flux estimation due to discrete integration procedure as well as stator resistance changes with variations in temperature. Several solutions to these problems are available and shall be considered in order to ensure continuous and reliable DTC drives operation [10].

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

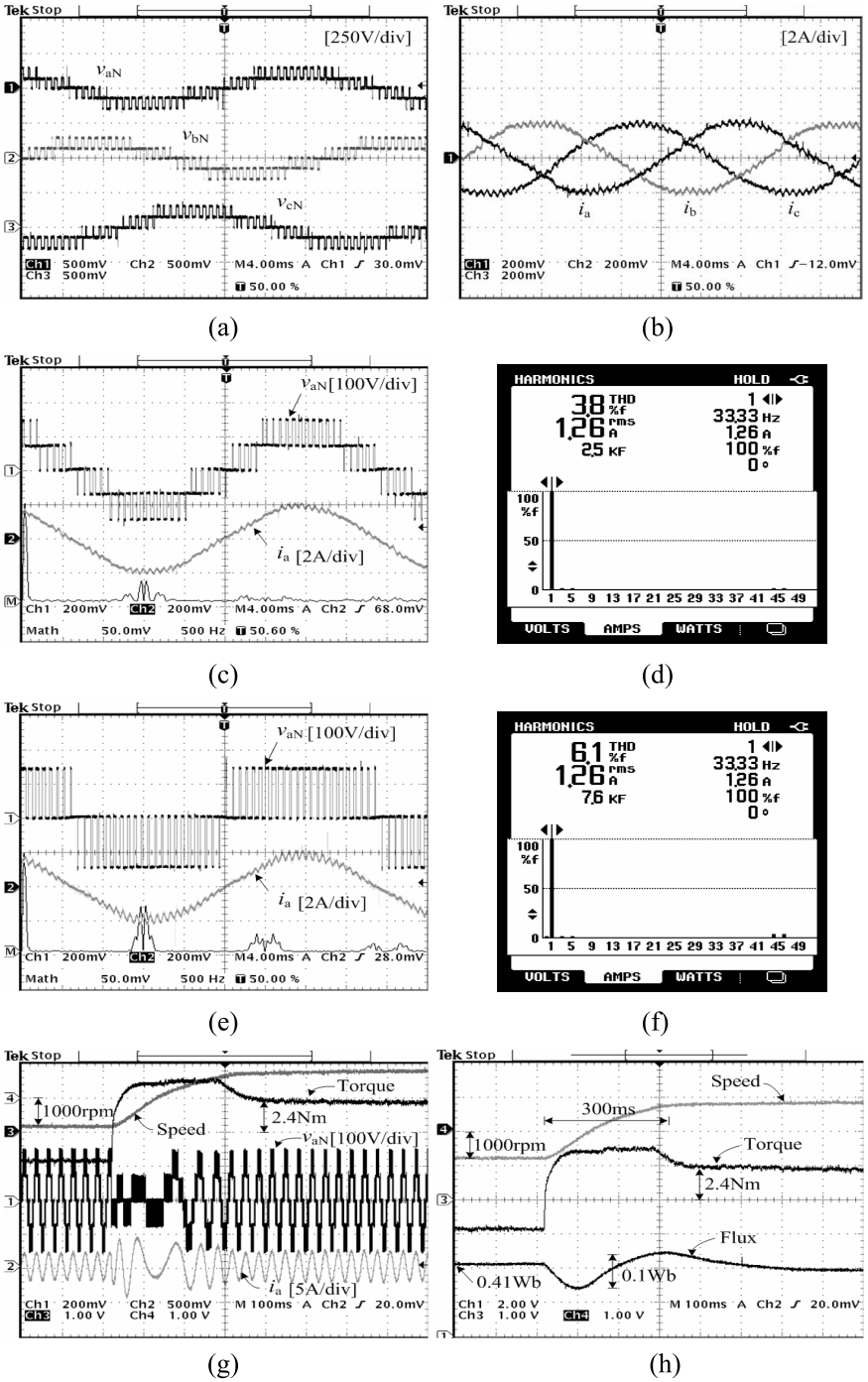

Fig. 3. Experimental results (a) Three-phase voltages of the proposed inverter (b) Three-phase currents of the proposed inverter (c) Phase A voltage and current waveforms of the proposed inverter (d) Current THD of the proposed inverter (e) Phase A voltage and current waveforms of three-level inverter (f) Current THD of three-level inverter (g) Voltage and current waveforms during speed reversal (h) Motor speed, torque and flux waveforms during speed reversal

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011

5 Experimental results and discussion

The proposed multilevel inverter was tested on a 1 kW 4-pole Baldor PMSM, BSM80C-2150. DTC algorithm and multilevel switching control were implemented using a digital signal processor (DSP) TMS320F2812. The DSP was chosen for its high-speed computation, suitable for complex algorithm motor control. The output current harmonics was observed on a Fluke 43B Power Quality Analyzer. The inverter's H-bridge part was built with 4 IGBTs, whereby the bidirectional switch from an IGBT with 4 power diodes. The capacitors, C_1 and C_2 were each 3400 μF. The inverter was supplied with dc link voltage, V_{dc} of 150 V. For PWM signal generation, the reference voltages were compared with the 1.5 kHz symmetrical triangular carrier. With multilevel output, low switching frequency is supported with comparable output quality, thus minimizes the switching losses. Sampling periods for DTC control loop and speed control loop were set to 50 μs and 0.5 ms respectively. The motor was run at 1000 rpm half rated speed and loaded with 2.4 Nm rated torque. Fig. 3 (a) and 3 (b) show the three-phase voltages and currents. Fig. 3 (c) and 3 (d) show five-level output waveforms with 3.8% current THD, which is very much lower than that of conventional three-level inverter with three phase H-bridge configuration having 6.1% THD as shown in Fig. 3 (e) and 3 (f). As can be seen, with multilevel output the current ripple has reduced. The inverter's functionality in running PMSM with DTC was verified by the speed reversal test results shown in Fig. 3 (g) and 3 (h). The figures show the dynamic changes in the motor speed, torque, flux, and the inverter's phase voltage and current during step changes in the speed reference. The torque and flux ripples are very low as a result of low current harmonics. The motor completes speed reversal in 300 ms where the flux magnitude changing is about 0.1 Wb in the transient. Fig. 3 (h) shows the developed torque during transient to be higher than rated torque, as the controller was designed to operate at 5 A rated peak current to achieve the desired speed faster.

6 Conclusion

In this paper, multilevel inverter based on single phase five-level topology for DTC drive is presented. The proposed inverter has reduced output harmonics, switching losses as well as power switches. The multilevel PWM signal was generated by comparing dual reference voltages and a symmetrical triangular carrier. The proposed inverter was compared with the conventional three-level inverter in terms of its output current THD, which was found to be much lower. The experimental results obtained show smooth changes in the motor speed, developed torque, stator flux, current and voltage, therefore verified its DTC-drive functionality.

DOI: 10.1587/elex.8.1
Received October 12, 2010
Accepted November 24, 2010
Published January 10, 2011