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A 5.5 mW 80–400 MHz Gm-C low pass filter with a unique auto-tuning system

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Abstract: A CMOS 80–400 MHz fifth order Chebyshev Gm-C low pass filter with a unique auto tuning system is presented. Both Gm and C are tuned digitally leading to a 5X tuning range. A digital magnitude-locked loop liked tuning system is proposed. The tuning system uses a digital calibration scheme, broadening the tuning range dramatically. A fifth order Chebyshev Gm-C filter with the proposed auto tuning system was designed with TSMC 0.13 μm RF CMOS process for verification. Measurement results show that the cut-off frequency of the filter can be tuned between 80–400 MHz, with an average tuning error of no larger than 3.6%. The dynamic range of the filter for THD less than 1% is 60 dB. The power dissipation is only 5.5 mW with 1.2 V supply voltage.

Keywords: filter, auto-tuning, wide tuning range, dynamic range

Classification: Integrated circuits

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1 Introduction

Applications like disk-drive/CD/DVD electronics require widely programmable high frequency anti-aliasing filters up to several hundred MHz. And integrated analog filters require automatic tuning circuits to correct deviation of the filter parameters due to aging, temperature and process variations.

The classical analog tuning method of Gm-C filters such as proposed in [2] is very simple but it has some drawbacks. Firstly, a control voltage needs to be applied to the transconductor in order to tune the Gm of the OTA. Since the control voltage has a limited swing, consequently the tuning range is limited. Secondly, the control voltage has to be hold, the tuning circuit always has to work, and the power consumption keeps large. In this work, a discrete tuning technique is presented. Both G_{m} and C are tuned to acquire a wide tuning range. A fifth order Gm-C filter is applied for verification, and the measurement results show an excellent performance of the filter and tuning circuits in the aspects of tuning range and accuracy, as well as the dynamic range and the power consumption.

2 Proposed auto tuning system and filter architecture

Fig. 1 (a) shows the proposed automatic-tuning system. Instead of applying a control voltage to the OTA, the proposed technique uses an N-bit data to control both the Gm and C. The lowest N-1 bit code is input to the N-1 binary weighted capacitance, and the highest bit to the transconductor. The OTA and the DCCA are replica of the transconductor and DCCA in the filter. The OTA is connected as a lossless integrator. The integrator's unity-gain is given by:

$$f_{\mathrm{u}} = \frac{G_{\mathrm{m}}}{2\pi C} \tag{1}$$

While $\mathrm{G_m}$ is the small signal transconductance of the OTA, and $\mathrm{C} = \mathrm{C_{min}} + \mathrm{b}^4 \cdot 2^4\Delta\mathrm{C} + \mathrm{b}^3 \cdot 2^3\Delta\mathrm{C} + \cdots + \mathrm{b}^0 \cdot 2^0\Delta\mathrm{C} = \mathrm{C_{min}} + n\Delta\mathrm{C}$.

Where

$$C_{\mathrm{min}} = \frac{C_{\mathrm{norm}}}{1+A} \tag{2}$$

$$\Delta C = \frac{2A}{(2^5-1)(1-A^2)} C_{\mathrm{norm}} \tag{3}$$

In the above equations, C_{norm} denotes the desired capacitance which is $C_{\mathrm{min}} + 2^4\Delta C$. '$A$' is the tuning range, which means that a time-constant variation within $1 \pm A$ can be tuned. Applying a reference signal $\mathrm{V_{REF}} = \mathrm{V}\sin(2\pi f_{\mathrm{r}}\mathrm{t})$, the output of the integrator becomes

$$V_{\mathrm{out}} = \frac{G_{\mathrm{m}}}{C_{\mathrm{L}}} \int V_{\mathrm{REF}} dt = \frac{f_{\mathrm{u}}}{f_{\mathrm{r}}} V \cos(2\pi f_{\mathrm{r}} t) \tag{4}$$

The amplitude of the integrator's output V_{out} is proportional to the ratio of the unity gain frequency f_{u} to the reference frequency f_{r}. Hence, by comparing the amplitude of the integrator's output and the reference frequency, the difference between the unity gain frequency and the reference frequency can be detected. The approach to compare the voltage is based on the com-

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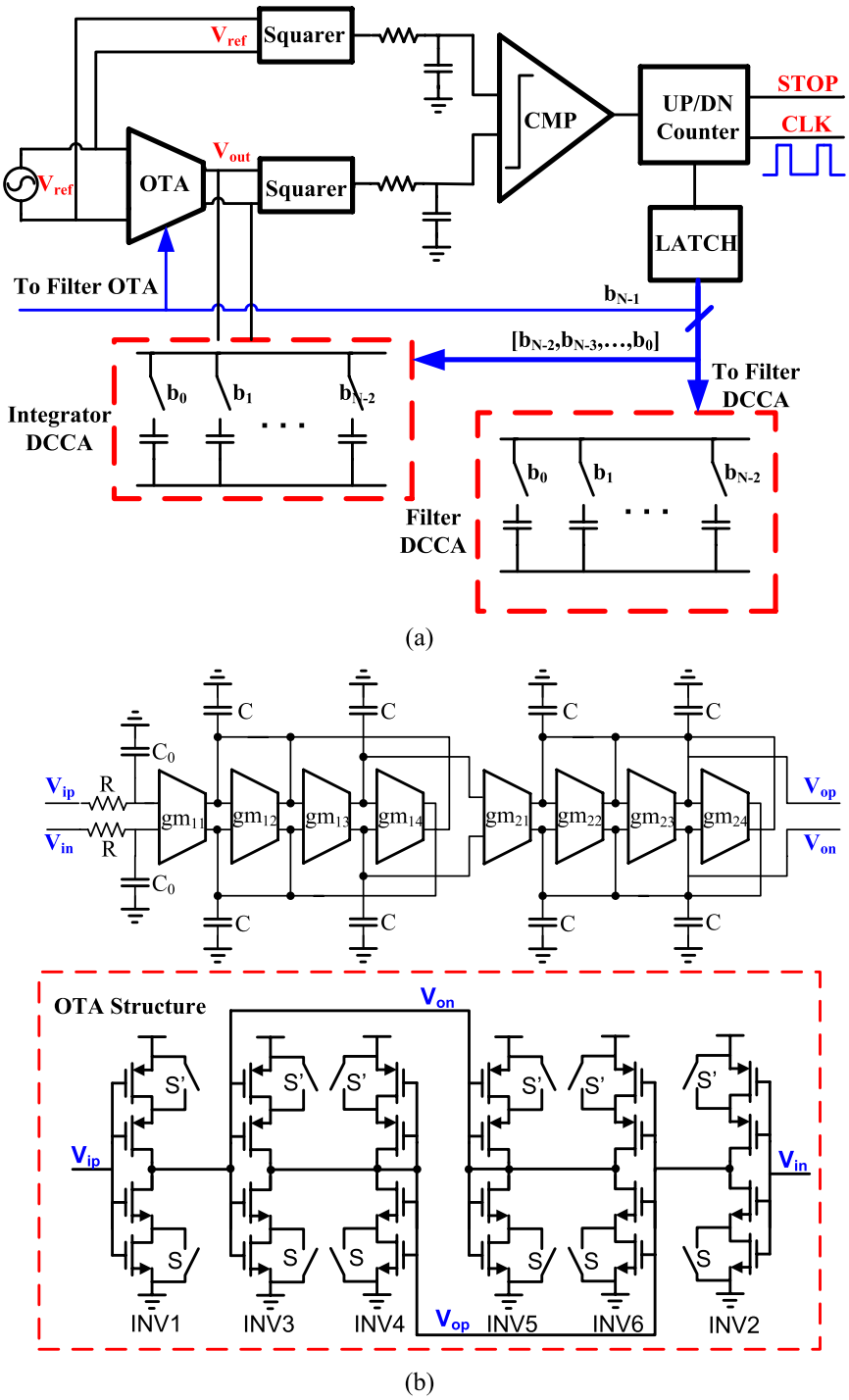

Fig. 1. (a) The proposed auto tuning system (b) The architecture of the proposed filter

parison of the mean squared values. Squaring V_{REF} and V_{out}, the following expressions can be obtained:

$$V_{\mathrm{REF}}^2 = \frac{V^2}{2} - \frac{V^2}{2}\cos(4\pi f_{\mathrm{r}} t) \tag{5}$$

$$V_{\mathrm{out}}^2 = \frac{V^2}{2}\left(\frac{f_{\mathrm{u}}}{f_{\mathrm{r}}}\right)^2 - \frac{V^2}{2}\left(\frac{f_{\mathrm{u}}}{f_{\mathrm{r}}}\right)^2 \cos(4\pi f_{\mathrm{r}} t) \tag{6}$$

Filtering out the high frequency components by the passive RC LPF, the

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dc levels are compared by a comparator and saved as a digital data, which indicate whether the unity gain frequency is larger or lower than the reference frequency. When the unity gain frequency of the integrator is higher than the reference frequency, the amplitude of the integrator's outputs is greater than the amplitude of the reference signal, comparator outputs high, while it outputs low in the opposite case. The N-bit UP/DOWN counter operates as the control circuit of binary-weighted capacitance and transconductance by changing the N-bit code $[b_{n-1}, b_{n-2}, \ldots, b_0]$. When the comparator outputs high, the counter up-counts on the rising edge of the CLK. The unity gain frequency of the integrator will be decreased. On the other hand, the counter down-counts and increases the integrator's unity-gain frequency. The counter's output is input into the integrator's cap array. Thus a negative feedback loop is formed, and the unity gain frequency can be tuned toward the reference frequency automatically.

The settling time is less than $2^N \cdot T_{CLK}$ while T_{CLK} is the period of the clock signal which can be set less than one hundred nanosecond. The worst case occurs when the initial code is $111\ldots11$ and the final code is $000\ldots00$ or vice versa. The main issue that determines the tuning error of this circuit is the quantum error. 'A $\pm$1 LSB' error occurs in the worst case because the final code will oscillate between the two codes. The quantum error can be derived from Equation (3) as follows:

$$Er = \frac{2A}{(2^5 - 1)(1 - A^2)} \tag{7}$$

In order to cover the entire frequency tuning range of 80–400 MHz, 'A' is set as 1/3, and the quantum error of 2.4% can be calculated. Moreover, the mismatch of 'Gm/C' in the tuning circuits and in the core filter circuit will also result in the tuning error. However, good layout can limit such mismatch to less than 1%. Thirdly, as described in the previous section, the comparator may output a wrong data if the difference between the input voltages is too small due to the DC-offset. Such DC-offset can also be minimized by the proper layout. According to the above analysis, the maximum tuning error of the proposed tuning technique will be less than 4%.

A fifth order low pass Gm-C filter is designed for verification. It is realized by a cascade of a one order RC filter and two biquads as illustrated in Fig. 1 (b). The transfer function of the biquad can be represented as:

$$H(s) = \frac{\frac{g_{m1}}{g_{m4}}\frac{g_{m3}g_{m4}}{C_1C_2}}{s^2 + s\frac{g_{m2}}{C_1} + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{8}$$

and the cut-off frequency of the filter is given by

$$\omega_c = \frac{g_{m3}g_{m4}}{C_1C_2} \tag{9}$$

In many cases, a programmable tranconductor is often used in Gm-C filters to achieve a wide tuning range. Using a parallel connection of transconductors is a feasible way to provide the function but dummy OTA is needed.

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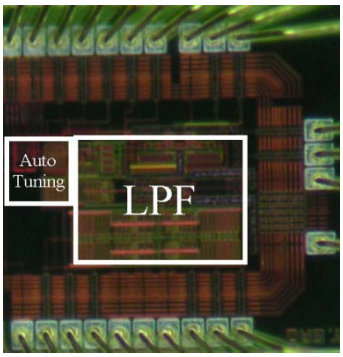
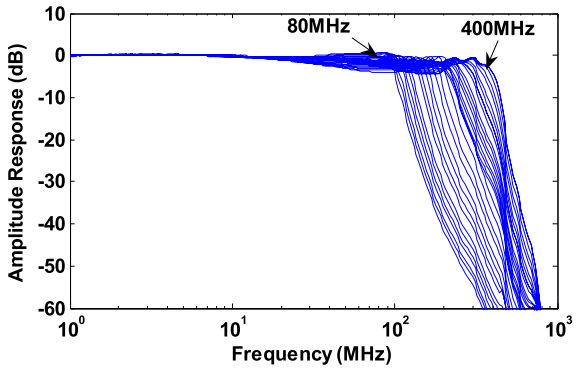
This will obviously cost a lot of power and area. In order to solve the problem, a modified Nauta's transconductor is come up with and presented in Fig. 1 (b). Each transistor in Nauta cell is split equally into two cells. So the length of each transistor is one half of the original one. When the switch S = 1, the OTA presented in Fig. 1 (b) becomes Nauta's structure, the transconductance of the OTA is G_m. When the switch S = 0, it becomes Gm/2. The power consumption can also be decreased by half. The modified Nauta G_m cell is implemented as the OTA in the filter. The transconductance of the all the OTA is controlled by a digital data b_5 simultaneously, the capacitance load is divided into a 5 bit binary weighted capacitance array.

3 Experimental results

The filter was designed with TSMC 0.13 μm CMOS process. The supply voltage is 1.2 V. The die photo of the designed LPF is shown in Fig. 2 (a). Die area of the filter is 0.16 mm^2. Measurement results show that the cut-off frequency of the filter can be tuned from 80 MHz to 400 MHz with an average tuning error of 3.6%, as illustrated in Fig. 2 (b). Power consumption is only



(a)



f_r (MHz)	90	100	200	300	350	380
f_u (MHz)	93	103	206	315	358	362
Error	3.3%	3.0%	3.0%	5.0%	2.3%	4.7%

(b)

Fig. 2. (a) The die photo of the filter (b) Frequency tuning range and tuning error of the proposed filter

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Table I. Performance Summary and Comparisons

	[3]	[4]	[5]	This Work
Technology (um)	CMOS 0.35	CMOS 0.13	CMOS 0.35	CMOS 0.13
Tuning Method	Analog	N/A	Digital	Digital
Tunable Elements	Gm	N/A	3 bits 'Gm'	5 bits 'Gm and C'
Filter Type	4^{TH} order Butterworth	5^{TH} order Chebyshev	4^{TH} order Butterworth	5^{TH} order Chebyshev
Bandwidth (MHz)	80-200	70-280	40-200	80-400
DR@THD<-40dB (dB)	52	53	58	60
Average Tuning Error	5%	N/A	4%	3.6%
Supply Voltage(V)	2.3	1.5	2	1.2
Power (mW)	72	21	9.6-48	3.5-5.5

5.5 mW. The performance summary and detailed comparisons are shown in Table I.

Compared with the digital tuning technique in [5], the proposed tuning scheme can achieve a wider tuning range, because both 'Gm' and 'C' are tunable and in [5] only 'Gm' can be tuned. It can also achieve higher accuracy because the capacitors can be better matched than OTAs. The proposed tuning circuit only contains one OTA while four OTAs are needed in [5], this leads to a less power consumption than [5]. The tuning scheme in [5] achieves a fine tuning by varying the biasing currents of the Gm, which will affect the performance of the filter. But the proposed tuning scheme varying the capacitors to achieve fine tuning, which will guarantee a good and stable performance of the filter.

4 Conclusions

A 5^{TH} order Chebyshev G_m-C filter with a digital magnitude locked loop liked auto tuning system is proposed. Both G_m and C are tuned in order to achieve a 5X tuning range. The proposed tuning technique is simple and flexible. The experimental results show that the filter can be tuned within 80–400 MHz, with a dynamic range of 60 dB and average tuning error of 3.6%. It also demonstrates a very low power consumption of maximum 5.5 mW from 1.2 V power supply.

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