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Phase-shift self-oscillating class-D audio amplifier with multiple-pole feedback filter

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Abstract: A self-oscillating class-D audio amplifier employing a multiple-pole feedback filter is introduced intended for portable multimedia devices. As the oscillation is based on the Barkhausen's criterion, the signal-dependent oscillation frequency is of great concern. Employing higher-order filters contributes to the stable oscillation frequency depending on the input amplitude as well as improves PSRR and THD. The concept is revealed comparatively with other works, and a design implemented in a 0.35 um CMOS process under 3.3 V supply is proposed and verified.

Keywords: PWM, class-D amplifier, self-oscillation, delta-sigma modulation

Classification: Integrated circuits

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1 Introduction

Class-D audio amplifier is increasingly replacing its classical analog Class-A

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and Class-AB counterparts due to the higher power-efficiency arising from the switching operation of the output stage. As it is inherently applicable to clocked systems, self-oscillating (SO) modulators for class-D audio amplifiers have been successfully integrated recently in three different modulation schemes, all requiring no reference clock signal.

The first one is the hysteresis-based modulation turning to a hysteresis window ($h = V_{DD}/V_{hyst}$) to constitute the oscillation frequency [1, 2]. Another one is the delay-based modulation including a time delay t_d around the loop [3]. It turns into an oscillation when the loop phase becomes 180°. The other method, the phase-shifting modulation, is made of a combination of poles and zeros [4]. It turns into an oscillation at the frequency satisfying the Barkhausen's criterion when the phase is 180° and the loop gain is unity.

However, these methods show a serious drawback of the non-constant switching frequency particularly depending on the input amplitude. The modulation index M is employed to assess its dependency [2], defined between $+1$ and -1 and related to the modulated duty-cycle D: $M = 2 \cdot D - 1$. The switching frequency decreases at high modulation index, causing the decrease of the out-of-band loop gain and the increase of the ripple noise at high frequencies [4]. The reduced loop gain, then, causes the increase of distortion (higher THD) and the degradation of PSRR in the closed-loop operation. On the other hand, the higher switching frequency than the target value causes unnecessary power consumption. Therefore, the fluctuation of the switching frequency is an important concern for mobile applications where low supply voltage and power consumption have the amplifier to be used often at its full excursion of signal amplitude.

It is reported that while the hysteresis and time-delay methods show the switching frequency variation depending on M^2, the phase-shifting modulation gets considerably reduced dependency [4]. Practically, the topology of phase shifting thus far is a hybrid type made of poles and the delay t_d. For such, this paper introduces a phase-shifting topology introducing two poles around the loop alleviating the additional attenuator. It achieves the better stability of switching frequency, improves PSRR, and reduces the effects of nonlinearities as well. Its analysis and implementation will be discussed.

2 Analysis of switching frequency variation

The architecture of the general phase-shift amplifier is shown in Fig. 1 (a). From the perspective of phase shift, it contains an integrator followed by an attenuator prior to the comparator, and the single-pole feedback filter. Fig. 1 (b) shows the corresponding linear model in the s-domain. To assess the PSRR of the modulator, the supply noise N_D is added at the output node. If the input and output variables in the summing node are regarded as currents, each block-level transfer function would be written as:

$$K_R = \frac{R_2}{R_1 + R_2}, \qquad A = \frac{1}{R_{in}}, \qquad G = -\frac{1}{sC} \tag{1}$$
$$H = \frac{1 + sC_2R_3}{R_3 + R_4 + sC_2R_3R_4} \cong \frac{1}{R_3 + R_4} \text{ (at low frequency)}$$

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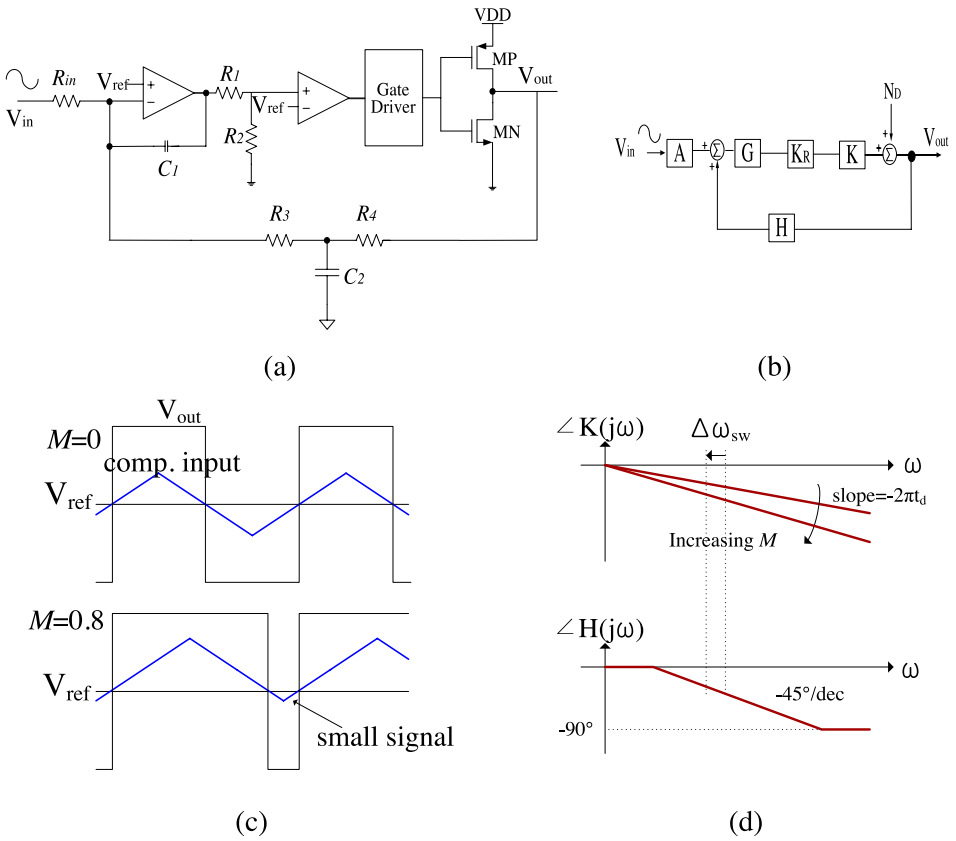

Fig. 1. Conventional modulator (a) architecture (b) linear block diagram in frequency domain (c) waveforms of comparator input at different Ms (d) signal-dependent (depending on M) shift of oscillation frequency

Therefore, the closed-loop transfer functions for the input signal and the supply noise (with low-frequency approximation) can be derived as follows:

$$A_f(s) = \left[\frac{V_{out}}{V_{in}}\bigg|_{N_D=0}\right] = -\frac{GAK_RK}{1+|G|K_RKH}$$
$$= -\frac{KR_2}{R_{in}C(R_1+R_2)}\left(\frac{1}{s+KR_2/C(R_1+R_2)(R_3+R_4)}\right) \cong -\frac{R_3+R_4}{R_{in}} \tag{2}$$

$$N(s) = \left[\frac{V_{out}}{N_D}\bigg|_{V_{in}=0}\right] = \frac{1}{1+|G|K_RKH} = \frac{s}{s+KR_2/C(R_1+R_2)(R_3+R_4)} \tag{3}$$

where K is the linearized gain of the comparator.

In the mean time, the oscillation criterion of the phase at the oscillation frequency f_{sw} is then described by (4)

$$\angle G(f_{sw}) = 90 + \left|\angle\frac{1}{1+j\cdot f_{sw}/f_{c2}}\right| + 360\cdot f_{sw}\cdot t_d \tag{4}$$

where f_{c2} is the pole frequency of the feedback filter above audio band, and t_d is the time delay mostly caused when passing through the comparator.

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The first term 90 comes from the phase shift of the integrator, the second term represents the phase shift through the feedback filter, and the last term is the phase expression of t_d. The modulator turns into an oscillation at the frequency f_{sw} where the phase sum reaches 180. Fig. 1 (c) shows waveforms at the comparator input for $M = 0$ (signal amplitude = 0), and $M = 0.8$ (80% of peak amplitude). Note that the greater probability of residing as a small signal near V_{ref} when $M = 0.8$ generates meta-stable operations more often that it brings about a greater delay through the comparator. It, then, shows a larger amount of phase shift by the third term of (4), and disturbs the switching frequency. As illustrated in Fig. 1 (d), the phase shift of K depending on M is buffered by H on the slope of $-45°$/decade, which leads to the signal-dependent variation of f_{sw}. Concerning about this setback of the signal-dependent oscillation frequency, an attenuator with R_1 and R_2 is employed to reduce the dynamic range of the comparator input so that the variation range of t_d can be limited.

3 Circuit design and simulation results

Fig. 2 (a) presents the proposed amplifier with multiple-pole feedback filter. From the perspective of phase shift, it contains a second-order integrator without the subsequent attenuator, a comparator, and the double-pole feedback filter. Fig. 2 (b) shows the corresponding linear model in the s-domain. The closed-loop transfer functions for the input signal and the supply noise (or quantization noise at the comparator) with the low-frequency approximation can be derived as follows:

$$\begin{aligned} A_f(s) &= \left[\frac{V_{out}}{V_{in}}\bigg|_{N_D=0}\right] = \frac{-GAK}{1+|G|KH} \\ &= -\frac{K}{R_{in}R_XC_1C_2}\left(\frac{1+sR_X(C_1+C_2)}{s^2+s\dfrac{(C_1+C_2)}{C_1C_2(R_1+R_2+R_3)}K+\dfrac{K}{C_1C_2R_X(R_1+R_2+R_3)}}\right) \\ &\cong -\frac{R_1+R_2+R_3}{R_{in}} \end{aligned} \tag{5}$$

$$\begin{aligned} N(s) &= \left[\frac{V_{out}}{N_D}\bigg|_{V_{in}=0}\right] = \frac{1}{1+|G|KH} \\ &= \frac{s^2}{s^2+s\dfrac{(C_1+C_2)}{C_1C_2(R_1+R_2+R_3)}K+\dfrac{K}{C_1C_2R_X(R_1+R_2+R_3)}} \end{aligned} \tag{6}$$

where K is the linearized gain of the comparator. The signal and noise transfer functions show the low-pass and high-pass filtering attributes, respectively. As these STF (signal transfer function) and NTF (noise transfer function) expose a nature of the delta-sigma modulation, a high switching frequency is desirable to enjoy advantages of high OSR (over-sampling ratio) in terms of SNR. However, it needs to be compromised by considering the

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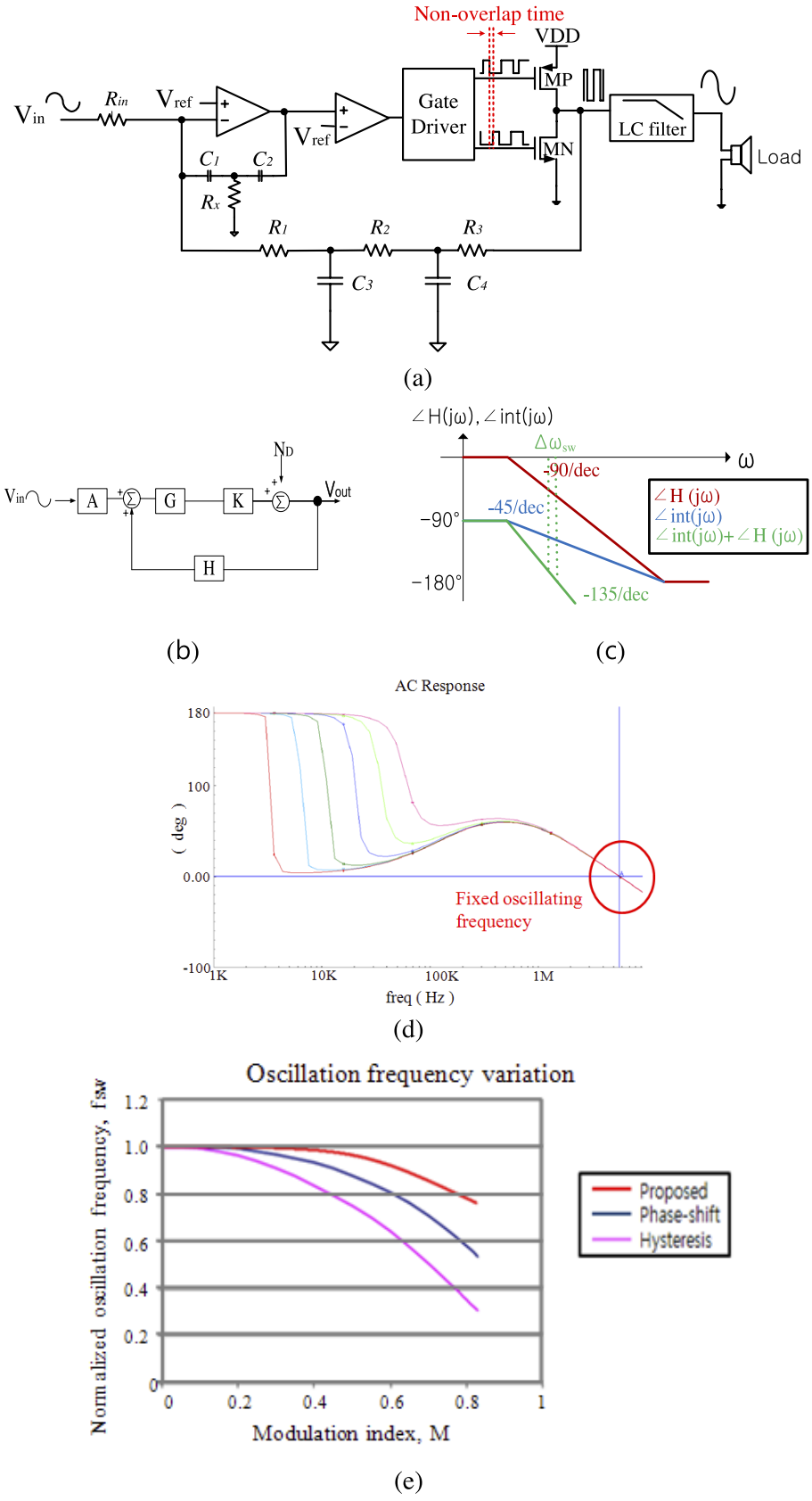

Fig. 2. Proposed modulator (a) architecture (b) linear block diagram in frequency domain (c) signal-dependent (depending on M) shift of oscillation frequency (d) composite phase response varying location of integrator poles (e) variation of oscillation frequency with respect to M

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switching power consumption with large parasitic capacitances. The oscillation criterion of the phase condition at the oscillation frequency f_{sw} is then described by (7)

$$\angle G(f_{sw}) = 90 + \left|\angle \frac{1}{1 + j \cdot f_{sw}/f_c}\right| + \left|\angle \frac{1}{1 + j \cdot f_{sw}/f_{c3}}\right| + \left|\angle \frac{1}{1 + j \cdot f_{sw}/f_{c4}}\right| + 360 \cdot f_{sw} \cdot t_d \quad (7)$$

where f_{c3}, f_{c4} are the pole frequencies of the feedback filter, f_c is the higher pole of the integrator above audio band, and t_d is the time delay which is mostly caused by the comparator propagation time. The first two terms come from the phase shift of the integrator, the second two terms represent the phase shift through the feedback filter, and the last term is mostly by propagation delay passing through the comparator.

Fig. 2 (c) illustrates the asymptotical phase responses of the integrator ($\angle$int) and the feedback filter ($\angle$H). It is postulated that the pole locations of the feedback filter, f_{c3} and f_{c4}, and the higher pole of the integrator f_c are at the very similar locations. On the other hand, the lower pole of the integrator is at near DC. The composite phase shift by three poles (two poles of the feedback filter and one pole of the integrator) is $-135°$/decade on the slope which is greater than the conventional $-45°$/decade on the single-pole (of the feedback filter) slope seen by (4). This steeper slope absorbs the signal-dependent variation of the comparator better than the conventional one, thus alleviates the need for an attenuator. As a result depicted in the plot, the disturbance of the switching frequency can be represented to be smaller depending on the input amplitude variation.

The proposed modulator was implemented in a 0.35 um-CMOS process with 3.3 V supply. As the switching transistors MN and MP have very small on-resistance over 0.4∼0.5 Ω, the dead time (non-overlap time) of about 1.35 ns was enforced to avoid the through current during the switching. The oscillation frequency is selected with $C_1 = C_2 = 400$ fF, $C_3 = C_4 = 600$ fF, $R_{in} = 100$ kΩ, $R_x = 1.5$ MΩ, $R_1 = 100$ Ω, $R_2 = R_3 = 300$ kΩ. An excursion of the signal amplitude could vary f_{sw} from 2.94 MHz ($M = 0.4$) to 3.06 MHz ($M = 0$).

Fig. 2 (d) shows the composite phase of the loop by Spectre simulations with the variation of the integrator poles. It can be noticed that the oscillation frequency is not so dependent on their locations. The comparative variation of the switching frequency according to M is simulated as shown in Fig. 2 (e). Several simulated points are smoothly connected in a curve for the proposed scheme while the curves of hysteresis and phase-shift are referenced to [4]. Table I shows the performance summary with different order of the integrator in the proposed scheme in conjunction with a prior work. The proposed scheme adopting the 2nd-order integrator shows a better performance than the 1st-order integrator.

4 Conclusion

The proposed self-oscillating scheme shows basically a delta-sigma nature,

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Table I. Performance comparison with prior works

	[4]	Proposed 1st order	Proposed 2nd order
Technology	0.25um	0.35um	0.35um
Supply voltage	2.3-5.5 V	3.3 V	3.3V
f_{sw} (M=0.8) / f_{sw} (M=0)	0.6	0.8	0.8
PSRR(dB)	65dB	69dB	74dB
SNR (dB)	91.7dB	112dB	123dB
THD + N (%)	-	0.0047%	0.0019%
Efficiency (%)	88%	90%	90%
Speaker load	8 Ω	8 Ω	8 Ω
Power consumption	3.88mA@3.6V	2.5mA@3.3V	2.5mA@3.3V
Active die area (㎟)	1.6 ㎟	0.6 ㎟	0.77 ㎟

leading to a higher oscillation frequency than the PWM method. While the higher-order loop gain contributes to the high PSRR and THD, the aspect of the stable oscillation frequency according to the input amplitude variation is particularly revealed. The validity of the proposed scheme is proved based on Spectre simulations using 0.35-um CMOS process. It achieved a PSRR of −74 dB at 1 kHz and a THD+N well below 0.0019% between 10 Hz and 20 kHz. The active chip area is 0.77 m^2 and the power consumption is 8.25 mW.

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