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A bandgap reference with resistance variation compensated

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Abstract: This paper describes a novel high-precision bandgap reference with resistance variation compensated. Novel process-compensated emitter current generator allows a substantial reduction on V_{BE} variation, resulting in an improved accuracy of the proposed bandgap reference. Comparison results in a 0.13 μm CMOS technology indicated that the proposed voltage reference achieved up to 62% improvement in terms of accuracy, as compared to conventional bandgap reference. Process variation of reference voltage is shown to be $\pm$3.67 mV for all process corners without any post-process trimming.

Keywords: bandgap reference, voltage reference, process compensation, process variation, V_{BE} generation

Classification: Integrated circuits

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1 Introduction

Bandgap reference has been widely used for generating a stable reference voltage in various analog and digital building blocks such as A/D and D/A

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converters, filters, DC-DC converters, and temperature sensors [1]. Any variation on the reference voltage affects the operating condition of these building blocks, resulting in performance degradation. The accuracy of the bandgap reference can be affected by the variation of integrated resistors. Hence, high-precision bandgap references [2, 3, 4] usually adopt a post-process trimming for compensating the variation. However, post-process trimming methods mandate additional processing cost, silicon area, and extra I/O pins for the embodiment and control of trimming circuits. To address these issues, this letter proposes a resistance variation-compensated bandgap reference for enhancing the accuracy without a post-process trimming. Section 2 describes the conventional bandgap reference and its limitations. Section 3 introduces the proposed bandgap reference. Comparison results are presented in section 4 to assess the performance of the proposed reference. Then, we draw our conclusion in section 5.

2 Conventional bandgap reference

Traditional bandgap reference for low-voltage operation is shown in Fig. 1 [2]. In this voltage reference, the temperature dependency of the reference voltage is compensated by summing the base-emitter voltage (V_{BE}) of a bipolar transistor and its difference (ΔV_{BE}) having opposite temperature dependencies. The reference voltage obtained by the bandgap reference can then be expressed as

$$V_{REF} = \frac{R_4}{R_2} \cdot \left(V_{BE} + \frac{R_2}{R_1} \cdot \Delta V_{BE} \right) \tag{1}$$

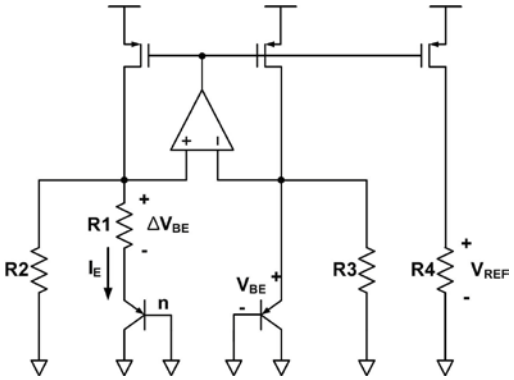

Fig. 1. Conventional low-voltage bandgap reference

when R_3 is assumed to be identical to R_2. Proper selection of R_1, R_2, and the area ratio of bipolar transistors, allows the term in the parenthesis to be independent upon the absolute temperature. Then, the value of R_4 can be properly chosen to put V_{REF} at an arbitrary value lower than 1.25 V [2]. In Equation (1), it looks that all the resistors used appear in a ratio form to minimize the effect of resistance variation. But, recognizing that I_E of the circuit in Fig. 1 is generated by R_1 applied with ΔV_{BE}, V_{BE} in Equation (1) can be represented as

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$$V_{BE} = V_t \ln\left(\frac{I_E}{I_S} \cdot \frac{\beta}{\beta+1}\right) = V_t \ln\left(\frac{\Delta V_{BE}}{R_1} \cdot \frac{1}{I_S} \cdot \frac{\beta}{\beta+1}\right) \quad (2)$$

As seen from Equation (2), V_{BE} is influenced by the variation of R_1. Since, in a typical CMOS technology, the process variation of a resistor is presented to be around $\pm 20\%$, the change of V_{BE} due to resistance variation can be very large. In our process, the resistance variation affects V_{BE} to change around $\pm 6.25\,\mathrm{mV}$. Likewise, since high-precision bandgap references in [3, 4] use a similar approach for biasing bipolar devices, unstable V_{BE} due to resistance variation inevitably presents a large variation on reference voltages.

3 Proposed bandgap reference

To eliminate resistance variation dependency of low-voltage bandgap references like the one in Fig. 1, the emitter current should not be generated on the basis of a resistor. The proposed bandgap reference utilizing an inverse relationship between the threshold voltage and k ($\mu_n C_{OX}$) of a MOS transistor [5] for emitter current generation is shown in Fig. 2 (a). It consists of a ΔV_{BE} generator, a V_{BE} generator, and a $\Delta V_{BE}/V_{BE}$ summer. In the V_{BE} generator, there is a process-compensated I_E generator, whose structure is

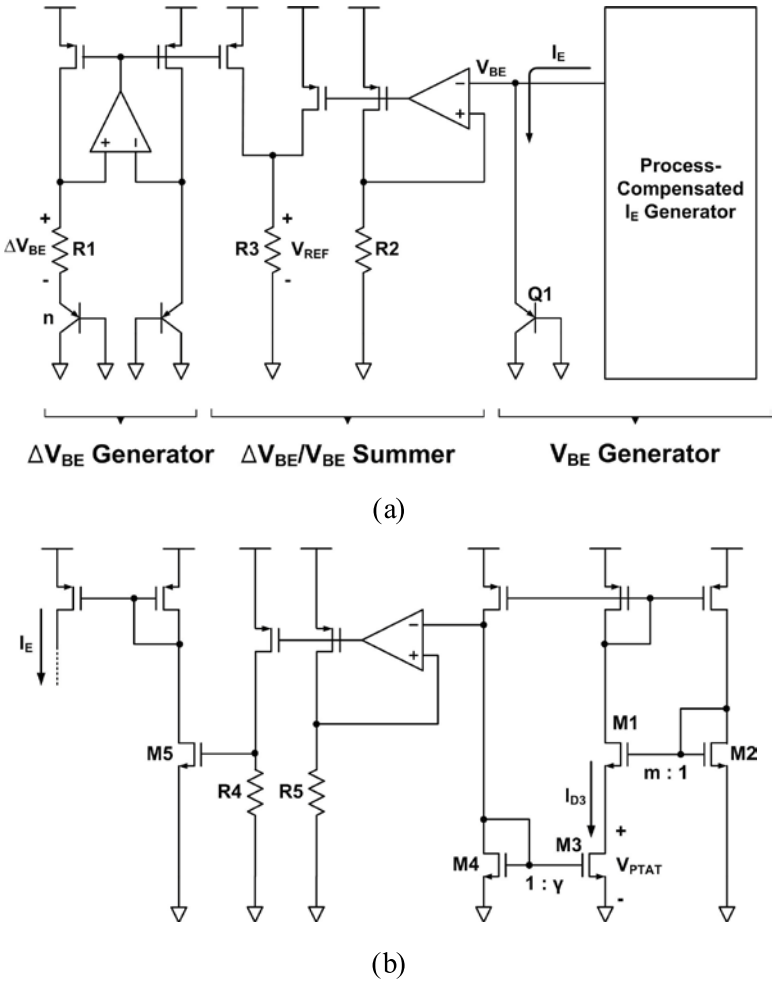

Fig. 2. Proposed bandgap reference: (a) overall structure, (b) process-compensated I_E generator

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shown in Fig. 2 (b). The drain current (I_{D3}) of M3 in Fig. 2 (b) is determined by the PTAT voltage across M1 and M2 operating in the weak-inversion region [6] and the on-resistance of M3 operating in the triode region, as shown in (3).

$$I_{D3} = \frac{V_{PTAT}}{R_{ON3}} = k \cdot (W/L)_{M3} \cdot (V_{GS3} - V_{TH}) \cdot V_{PTAT} \tag{3}$$

The drain current (I_{D4}) of diode-connected M4 can also be written as

$$I_{D4} = \frac{1}{2} k \cdot (W/L)_{M4} \cdot (V_{GS4} - V_{TH})^2 \tag{4}$$

Recognizing that $I_{D3} = I_{D4}$ and $V_{GS3} = V_{GS4}$ as seen in Fig. 2 (b), by combining Equations (3) and (4), V_{GS4} of M4 can be expressed as

$$V_{GS4} = V_{TH} + 2\gamma \cdot V_{PTAT} \tag{5}$$

where γ is the device size ratio between M3 and M4. Equation (5) indicates that V_{GS4} is presented as the sum of a scaled PTAT voltage and an MOS threshold voltage. Then, after being multiplied by resistor ratio, R4/R5, V_{GS5} of M5 can be expressed as

$$V_{GS5} = \frac{R_4}{R_5}(V_{TH} + 2\gamma \cdot V_{PTAT}) \tag{6}$$

Then, the emitter current fed into Q1 in Fig. 2 (a), which is generated by M5, can be expressed as

$$\begin{aligned} I_E &= I_{D5} \\ &= \frac{1}{2} k \cdot (W/L)_{M5} \cdot (V_{GS5} - V_{TH})^2 \\ &= \frac{1}{2}(k_0 + \delta k) \cdot (W/L)_{M5} \cdot \left[\left(\frac{R_4}{R_5} - 1\right) \cdot (V_{TH0} + \delta V_{TH}) + 2\gamma \cdot \frac{R_4}{R_5} \cdot V_{PTAT}\right]^2 \end{aligned} \tag{7}$$

Now, considering the inverse relationship between V_{TH} and k in terms of process variation, I_E can be made to have its V_{TH} and k variations cancelled from each other, and will be process-independent when a condition of

$$\left|\frac{k_0 + \delta k}{k_0}\right| \cdot \left|\frac{\left(\frac{R_4}{R_5} - 1\right) \cdot V_{TH0} + 2\gamma \cdot \frac{R_4}{R_5} \cdot V_{PTAT} + \left(\frac{R_4}{R_5} - 1\right) \cdot \delta V_{TH}}{\left(\frac{R_4}{R_5} - 1\right) \cdot V_{TH0} + 2\gamma \cdot \frac{R_4}{R_5} \cdot V_{PTAT}}\right|^2 = 1 \tag{8}$$

is satisfied under proper values of R4/R5 and γ. With this process-compensated emitter current (I_{E_COMP}), the base-emitter voltage of Q1 can be expressed as

$$V'_{BE} = V_t \ln\left(I_{E\_COMP} \cdot \frac{1}{I_S} \cdot \frac{\beta}{\beta + 1}\right) \tag{9}$$

Since the base-emitter voltage is now compensated for the emitter current variation, the variation of the voltage is significantly reduced. Adding ΔV_{BE} and V_{BE} by the $\Delta V_{BE}/V_{BE}$ summer in Fig. 2 (a), the reference voltage can be expressed as

$$V'_{REF} = \frac{R_3}{R_2} \cdot \left(V'_{BE} + \frac{R_2}{R_1} \cdot \Delta V_{BE}\right) \tag{10}$$

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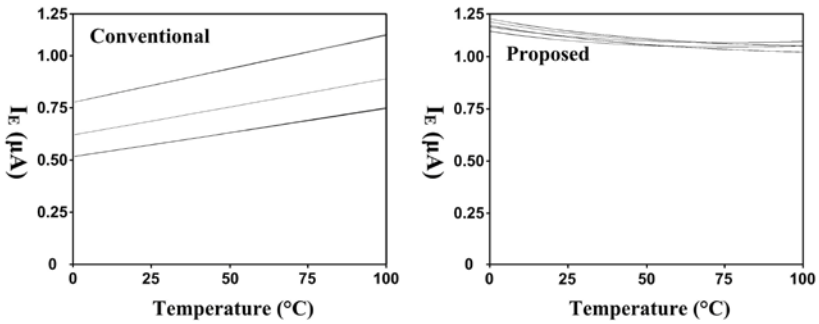
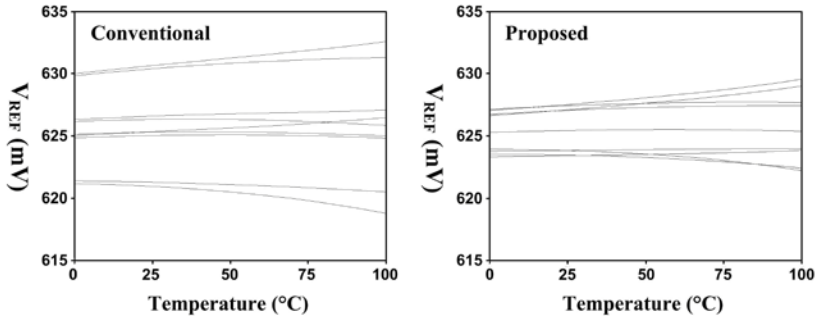
As seen in (10), the reference voltage of the proposed bandgap reference is determined by the base-emitter voltage having reduced process variation, ΔV_{BE} having no process variation, and the ratio of resistors whose process dependency can be minimized by proper matching. Therefore, the accuracy of the proposed voltage reference is considerably improved, as compared to that of the conventional voltage reference.

4 Comparison results

To assess the performance of the proposed scheme, the conventional and proposed voltage references were designed in a 0.13 μm CMOS technology. Performance comparison for these references was performed with a supply voltage of 1.2 V for a temperature range of 0 to 100°C. Fig. 3 (a) depicts temperature versus emitter current relationship at various process corners. For the conventional bandgap reference in Fig. 1, the emitter current shows



(a)



(b)

Parameter	Banba [2]	Leung [3]	Malcovati [4]	Proposed
Process error (mV)	±6.96mV	±9.69mV	±7.10mV	±3.67mV
Curvature error (ppm/°C)	118	15	19	5
Process technology (μm)	0.40	0.60	0.80	0.13
Min. supply voltage (V)	2.1	0.98	0.95	0.96
Temperature range (°C)	27~125	0 ~ 100	0 ~ 80	0~100
Operating current (μA)	2.2	18	92	28

(c)

Fig. 3. Comparison results: (a) temperature versus I_E graphs in terms of process variation, (b) temperature versus V_{REF} graphs in terms of process variation, (c) performance summary

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a large process dependency, indicating as much as ±20% variation. For the proposed bandgap reference, the current generated shows a significantly reduced process dependency, indicating under ±3% variation. Fig. 3 (b) shows temperature versus V_{REF} graphs of the conventional and proposed bandgap references in terms of process variation. The proposed voltage reference significantly improves the immunity to process variation as compared to the conventional voltage reference. Performance summary of voltage references is shown in Fig. 3 (c). For a fair comparison, process errors of the bandgap references are obtained by simulations at the all process corners with an identical reference voltage of 625 mV. The accuracy of the proposed bandgap reference indicates ±3.67 mV for process variation, presenting up to 62% improvement as compared to the conventional voltage reference. Improved accuracy of the proposed bandgap reference allows no use of post-process trimming, resulting in cost reduction due to no extra processing steps, reduced silicon budget, and no extra I/O pins for trimming.

5 Conclusion

In this paper, a novel bandgap reference adopting a process-compensated emitter current generator is presented for improving the accuracy of the reference voltage. Evaluation in a 0.13 μm CMOS technology indicated that the proposed bandgap reference achieved up to 62% improvement on the immunity to process variation as compared to conventional voltage references. Therefore, the proposed bandgap reference is well suited for low-cost medium-precision application.

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