ELectronics EXpress

IEICE Electronics Express, Vol.8, No.3, 182–188

Microprocessor power noise measurements with different levels of resource occupancy

Yoji Bando[a)] **and Makoto Nagata**[b)]

Graduate school of system informatics, Kobe university

1–1 Rokkodai-cho, nada-ku, Kobe 657–8501, Japan

a) *bando@cs26.scitec.kobe-u.ac.jp*

b) *nagata@cs.kobe-u.ac.jp*

Abstract: Power noise waveforms of a 32-bit microprocessor were on-chip measured in a 90-nm CMOS technology. A dedicated measurement system combines an embedded programming environment and a measurement flow that ensures acquisition of noise waveforms during designated arithmetic operation. Power noise exhibits clear relation with the contents of computation, where the magnitude of power noise reflects the occupancy ratio of computing resources of a microprocessor. The level of correlation is shown to be different among static and dynamic portions of power noise. It is concluded that practical power noise analysis requires the higher-level abstraction of a large-scale integrated digital system.

Keywords: power integrity, signal integrity, dependability, resiliency

Classification: Integrated circuits

References

[1] R. Saleh, S. Z. Hussain, S. Rochel, and D. Overhaser, "Clock Skew Verification in the Presence of IR-Drop in the Power Distribution Network," *IEEE Trans. Computer-Aided Design Integr. Circuits Syst.*, vol. 19, no. 6, pp. 635–644, June 2000.

[2] T. Rahal-Arabi, G. Taylor, M. Ma, and C. Webb, "Design and Validation of the Pentium III and Pentium 4 Processors Power Delivery," *Dig. Tech. Papers, 2002 Symp. VLSI Circuits*, pp. 220–223, June 2002.

[3] T. Sato, Y. Matsumoto, K. Hirakimoto, M. Komoda, and J. Mano, "A Time-Slicing Ring Oscillator for Capturing Instantaneous Delay Degradation and Power Supply Voltage Drop," *Proc. Custom Integrated Circuits Conf.*, pp. 563–566, Sept. 2006.

[4] T. Matsuno, D. Kosaka, and M. Nagata, "Modeling of Power Noise Generation in Standard-Cell Based CMOS Digital Circuits," *IEICE Trans. Fundamentals*, vol. E93-A, no. 2, pp. 440–447, Feb. 2010.

[5] Y. Bando, S. Takaya, and M. Nagata, "An On-Chip Continuous Time Power Supply Noise Monitoring Technique," *Proc. IEEE Asian Solid-State Circuits Conference 2009*, pp. 97–100, Nov. 2009.

[6] Y. Kanno, Y. Kondoh, T. Irita, K. Hirose, R. Mori, Y. Yasu, S. Komatsu, and H. Mizuno, "In-Situ Measurement of Supply-Noise Maps With Milli-

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

volt Accuracy and Nanosecond-Order Time Resolution," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 784–789, April 2007.

[7] M. Fukazawa, M. Kurimoto, R. Akiyama, H. Takata, and M. Nagata, "Experimental Evaluation of Dynamic Power Supply Noise and Logical Failures in Microprocessor Operations," *IEICE Trans. Electron.*, vol. E92-C, no. 4, pp. 475–482, April 2009.

1 Introduction

Power noise is considered as a source of dynamic environmental variability, impacting operation of very large scale integrated (VLSI) circuits [1, 2]. Physical origins of power noise widely range from device-level principles to system-level behavior. In the present paper, we focus on the variation of power noise in a microprocessor, exhibiting close relation with the level of occupation of computational resources.

Power noise of a digital integrated circuit has been almost investigated in the simple array or groups of logic gate elements [3, 4], where transistor-level operation of a circuit is microscopically connected with power noise generation and its impacts. However, the relation of power noise with digital processing contents, that will be a real basis of the understanding of environmental variability in a large scale digital system, is still unclear in those experiments.

An on-chip power noise monitoring technique captures continuous-time power noise waveforms in a digital circuit [5]. This technique is applied to a 32-bit microprocessor in the present work and evaluates its noise characteristics. This is the first test case that can provide a general picture of power noise generation of a microprocessor with close connection to the contents of computation, with the support of embedded programming.

2 Test environment

A prototype chip of Fig. 1 was fabricated in a 90-nm CMOS technology. On-chip continuous-time monitor (OCM) circuits are arrayed along the periphery of a 32-bit microprocessor (μP) and their probe wirings are drawn to the internal nodes of interest on power (Vdd) and ground (Vss) planes.

The chip incorporates 14 OCM circuits, provided a pair of Vdd and Vss probe wirings for each circuit. Probe points are evenly distributed on the power planes. Power noise in the center of μP is evaluated in the present paper, where signals with high activities are concentrated. Another pair of wirings is connected to an external signal port for the purpose of calibration of monitor response.

The array of OCM circuits is located along the side of μP and between I/O arrays and μP. This facilitates the wirings to be drawn into the probe points of interest, and also minimizes the length of wirings at the output. The OCM circuits are separately supplied by $\mathrm{Vdd_{ocm}}$ and $\mathrm{Vss_{ocm}}$, and isolated from I/O arrays as well as μP by dedicated p+ guard rings. These layout

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

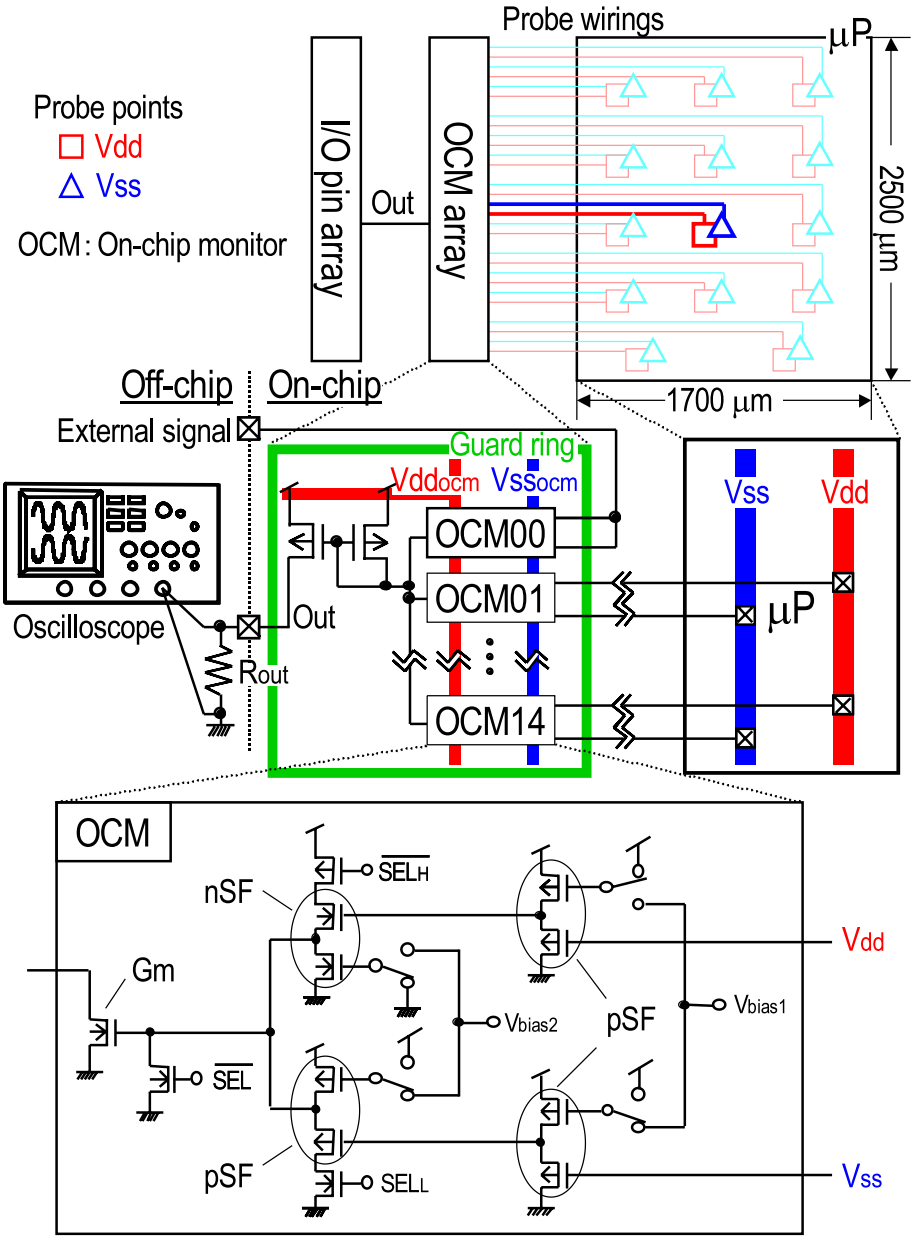

Fig. 1. Prototype chip for power noise measurements.

techniques are expected to suppress background power noise coupling into OCM circuits.

The OCM circuit, shown in the inset of Fig. 1, accommodates a pair of input channels for sensing voltage variation on Vdd and Vss [5]. The input voltage at Vss is sensed and shifted twice upward by a cascade of two p-channel source followers (pSF) in Vss branch. On the other hand, the input voltage at Vdd is sensed by a cascade of p- and n-channel source followers that offset voltages compensate each other, in Vdd branch. These Vdd and Vss branches are designed to have mostly equivalent DC voltage at the connection node to a subsequent n-channel common-source transistor (Gm). One of the branches is selectively activated and sensed voltage is converted into current by Gm. This current is then buffered by a current

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

mirror circuit and flows to an off-chip termination resistor, Rout. A voltage waveform generated on Rout is captured by an oscilloscope, as continuous-time reproduction of voltage variation seen at the selected node of interest. All the probing branches are deactivated except for a single branch that is intentionally selected.

A power noise measurement system of Fig. 2 was constructed, featuring a tight connection of the prototype chip and an embedded programming environment of a microprocessor. This allows quantitative evaluation of power noise in response to known contents of digital processing and provides advantages over the past works [6, 7] for the purpose of understanding power noise generation in a VLSI system.

The measurement procedure is as follows. The μP is initialized at the beginning, and then a program of arithmetic operations and a set of input variables are stored in an on-die user memory of the test chip through JTAG interface. The operation is repeated for a certain number of times with the same input variables, and then the result of computation is compared with an expected value for verification. The entire loop continues with a new set of input variables one after another, as long as the comparison does not fail. On-chip waveforms are captured during the iterative operations, where an oscilloscope is triggered by a return-to-zero (RZ) pulse that is asserted by the μP at the every entry to the loop. Therefore, this procedure ensures that the derived power noise information is directly related to the nature of individual arithmetic operations.

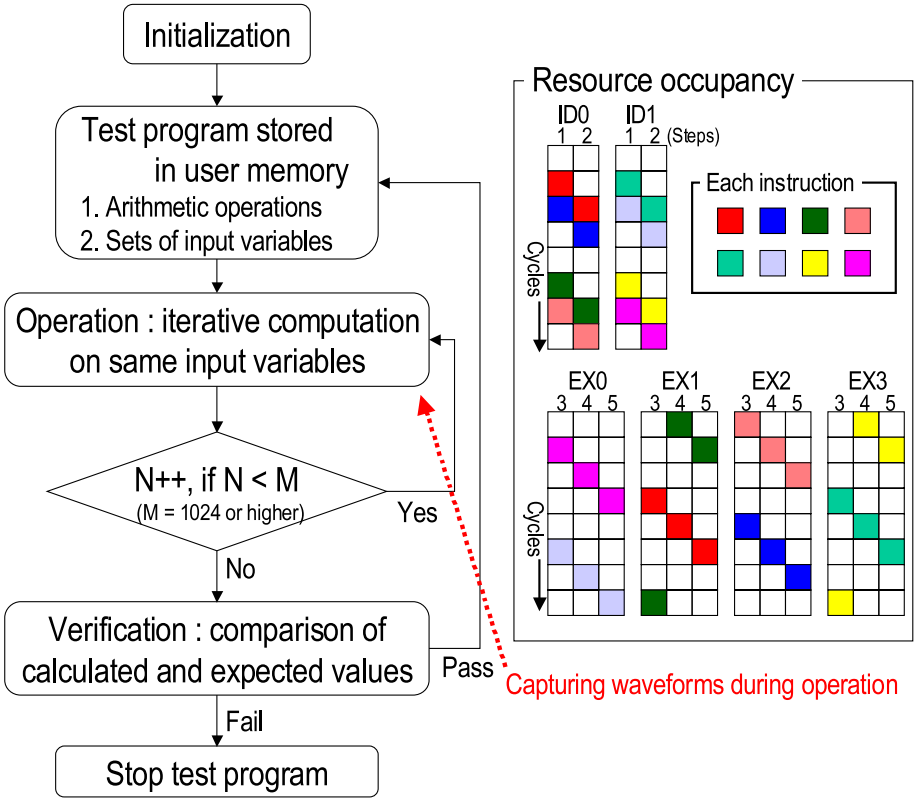

Fig. 2. Microprocessor power noise measurement flow.

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

We have developed the test programs in an embedded programming environment, considering the level of occupation of computation resources. The μP is based on a five-stage pipeline and two-way super scalar RISC architecture, and equipped with four execution modules EX0, EX1, EX2, EX3 that can be issued in parallel. The execution modules include such as arithmetic logical units that are prepared separately for integer and floating point operations, and memory access paths. While two instructions are fetched and decoded at the same time among the two-way super scalar modules of ID0, ID1, the instruction-level parallelism (ILP) among the execution modules depends on operands as well as opcodes.

We define the ratio of occupancy as (1) for this μP. The #nn stands for the number of clock cycles of individual modules occupied by a single arithmetic operation, where the total clock cycles of ALL is consumed. Power noise will be evaluated with regard to the occupancy of the μP.

$$Occupancy = \frac{\#ID0 + \#ID1 + \#EX0 + \#EX1 + \#EX2 + \#EX3}{6 \cdot ALL} \quad (1)$$

Test programs are designed for different levels of occupancy as well as various combinations of computation resources to occupy. While the higher ILP will create the larger occupancy, the conflicts among operands or execution modules may cause stalls in pipeline operation and reduce the occupancy. The embedded programming environment strongly helps the design of our test programs since the operation is resolved at the machine-language level for the purpose of hardware-level debugging.

3 Power noise evaluation

Power noise information is derived for forty test programs, as summarized in Fig. 3. The first column shows the occupancy of individual test programs calculated by (1). The horizontal axis shows the identification (ID) number of the test programs, labeled in the order of occupancy. The test programs are designed to cover a wide range of occupancy, however, the level of occupancy is often identical among programs even with the different usage of execution modules.

Average power current (I_{vdd}) is given in the second column, measured by an ampere meter of an off-chip power source. The continuous iteration of a particular arithmetic operation is needed for the integration time of the meter. It is almost natural that the larger power current is consumed for the higher occupancy, however, there are some exceptions such as test ID of 39 and 40. It is considered that the execution modules with smaller internal logic activity are occupied.

By using on-chip continuous-time monitors, static voltage drops (Vst) and dynamic voltage variations (V_{pk2pk}) are evaluated on Vdd and Vss planes. The third column compares static drops, Vst, among test programs. The size of Vst for Vdd and Vss are measured from the nominal supply voltage of 1.0 V and ground voltage of 0.0 V, respectively. Comparing the second and third columns, the size of voltage drop naturally follows to the average

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

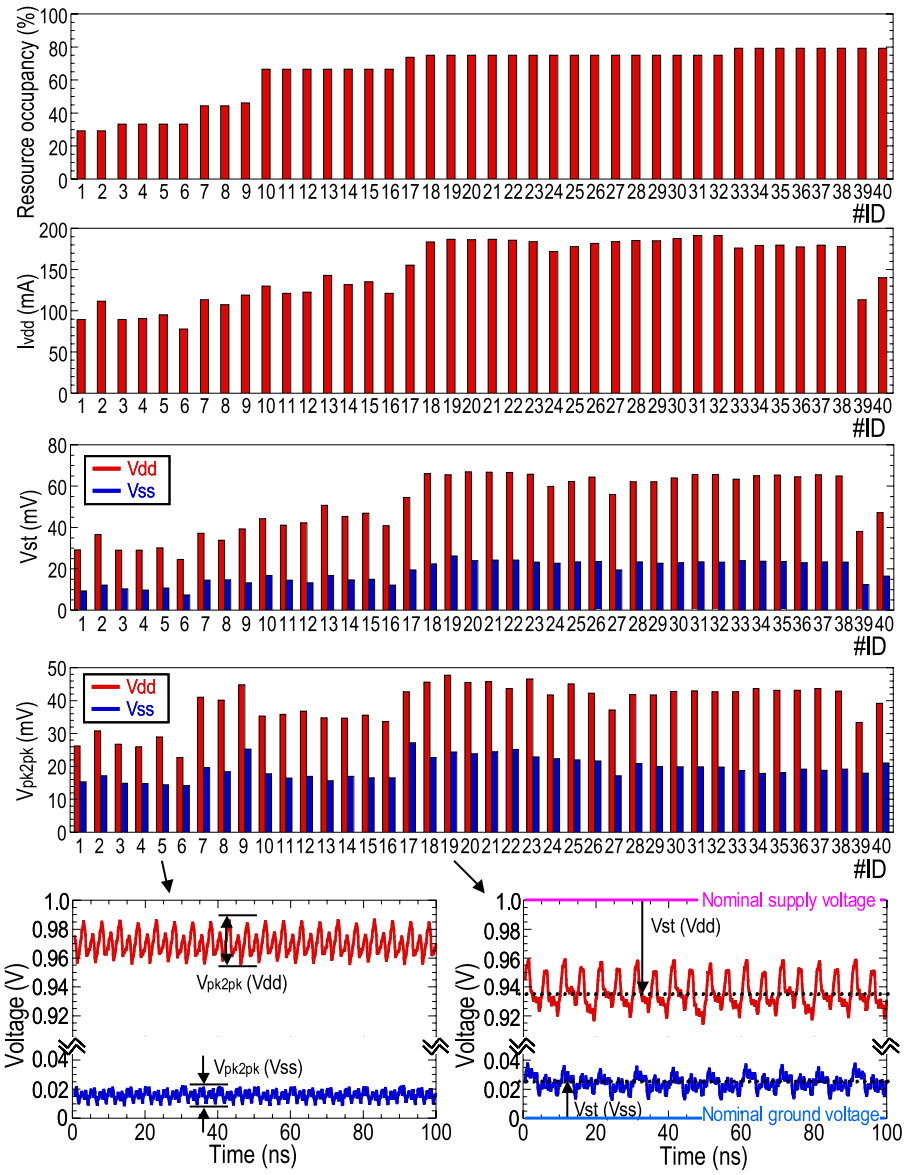

Fig. 3. Measured power noise with relation to occupancy of computation resources.

power current. This is due to the fact that the current flows through series resistance parasitic to power lines. The resistance on Vdd and Vss are derived as Rvdd = 0.34 Ω and Rvss = 0.12 Ω, respectively. The smaller Rvss results from connections of multiple Vss pads through a resistive substrate.

The fourth column plots the size of peak-to-peak voltage variation, V_{pk2pk}, extracted from the waveforms. It is of particular interest that the correlation of V_{pk2pk} and the occupancy of computation resources is not lost but becomes weaker, compared to Vst. The V_{pk2pk} represents a variety of aspects of the design of the μP, in contrast to the leveled power noise characteristics such as Vst. Logical depths and delays among logical data paths, distribution of skews and jitters in clocking networks, non-uniformity of power supply grids, and so on, are throughly involved in the formulation of dynamic voltage variation.

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011

The fifth column demonstrates examples of power noise waveforms, and gives the definition of Vst and V_{pk2pk}. Voltage and timing resolution of a waveform measurement is 100 μV and 400 ps, respectively, defined by an external oscilloscope. The dynamic change of voltage is apparently synchronous to the clock signal of μP at 200 MHz.

4 Conclusion

Dynamic power noise waveforms are experimentally evaluated against the occupation of computing resources in a microprocessor. It is apparently exhibited that the size of voltage variation is closely related to the contents of computation. Considering the limited capacity of device-level simulation, power noise analysis at the higher level of abstraction is obviously necessitated for computer simulation of these results. This is a technology challenge for the future, and will provide a solid design solution against the dynamic environmental variability of a large-scale digital system.

Acknowledgements

The authors would like to thank Yuya Nishihara.

DOI: 10.1587/elex.8.182
Received December 31, 2010
Accepted January 07, 2011
Published February 10, 2011