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A test pattern generation method with high compression ratio

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Abstract: This paper proposes a test pattern generation and compression method to reduce test volume for VLSI testing. Unlike traditional approaches, the proposed scheme predefines linear relationships between vectors or within a vector of a test sequence firstly. Then, it determines test patterns by fault simulation. Therefore, patterns of a deterministic test set keep the predefined linear relationships, and can be highly compressed. Simulation results on ISCAS'89 benchmarks demonstrate that the proposed method can significantly reduce the data size with high fault coverage.

Keywords: test pattern generation, test compression, linear relation

Classification: Integrated circuits

References

[1] A. Chandra and K. Chakrabarty, "Test data compression and test resource partitioning for system-on-a-chip using frequency-directed run-length (FDR) codes," *IEEE Trans. Comput.*, vol. 52, no. 8, pp. 1076–1088, Aug. 2003.

[2] S. Mitra and K. S. Kim, "XPAND: an efficient test stimulus compression technique," *IEEE Trans. Comput.*, vol. 55, no. 2, pp. 163–173, Feb. 2006.

[3] Z. Chen, S. Seth, D. Xiang, and B. B. Bhattacharya, "A Unified Solution to Scan Test Volume, Time, and Power Minimization," *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, pp. 9–14, 3-7 Jan. 2010.

[4] X. Kavousianos, E. Kalligeros, and D. Nikolos, "Multilevel-Huffman test-data compression for IP cores with multiple scan chains," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 16, no. 7, pp. 926–931, July 2008.

[5] K. Basu and P. Mishra, "Test data compression using efficient bitmask and dictionary selection methods," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 9, pp. 1277–1286, Sept. 2010.

1 Introduction

For multiple parallel scan chains, test volume and test time usually grow quickly with the circuit under test (CUT)'s size. So test compression has been

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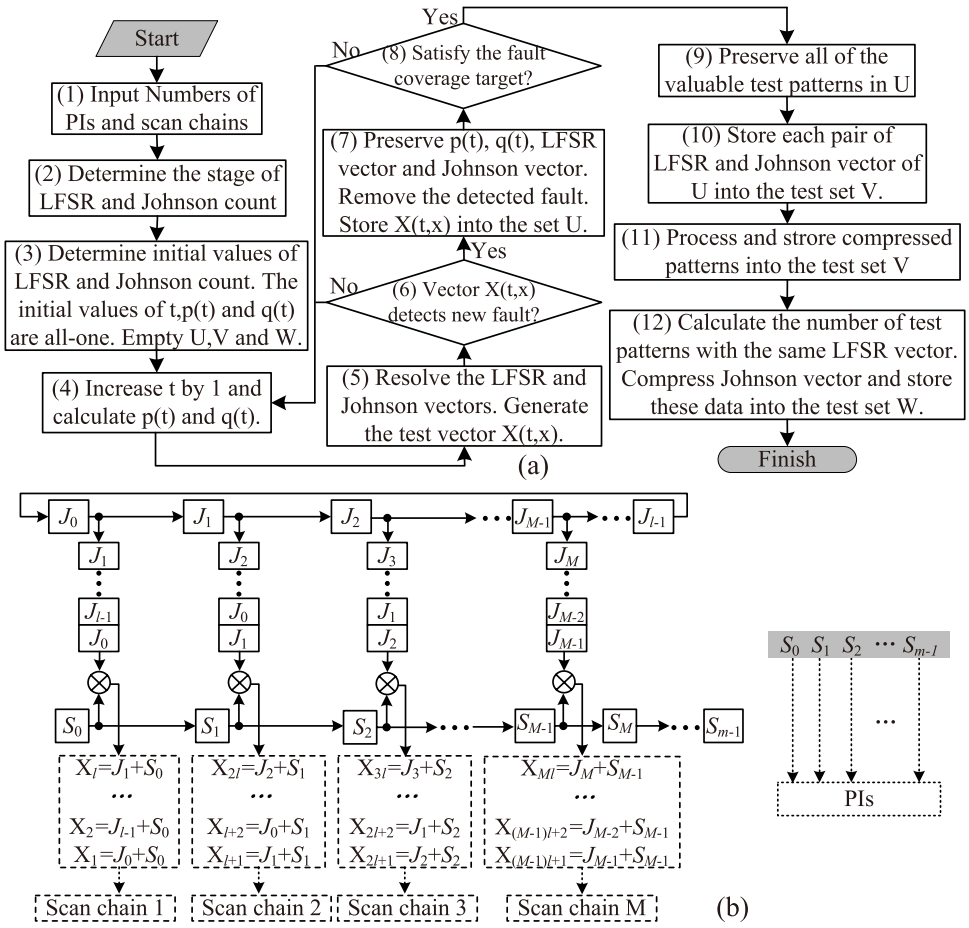

Fig. 1. (a) Flow chart of the HC algorithm (b) Symbolic representation of a HC pattern for scan chains

an important research topic. Test compression schemes fall broadly into three categories: code-based schemes [1], linear-decompression-based schemes [2] and broadcast-scan-based schemes. This paper proposes a novel ATPG (automatic test pattern generation) and compression technique. In section 2, it describes the generation method of the highly compressible test sequence and its characteristics. Section 3 presents the compression algorithm and decompression mechanism. Experiment results are showed in Section 4. Section 5 concludes this paper.

2 Principle of the highly compressible test sequence

Fig. 1 (a) illustrates the proposed test generation flow. It can be divided into two phases:

Phase 1—Test patterns generation. Step 1 to step 9 find a class of test sequences which is called the highly compressible (HC) test sequence in this paper. At time t, a vector of the test sequence is the bitwise exclusive OR result of an LFSR vector and a Johnson vector, and p(t) and q(t) are used as labels to record sequence numbers of valuable test vectors. The value of $q(t)$ is increased every clock cycle, and the value of $p(t)$ will be increased once when q(t) equals 2 times of Johnson count stage. That is, the LFSR

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sequence will change once after the Johnson sequence is generated. We can consider the LFSR vector as a seed vector. More definitions about p(t) and q(t) can be found in Section 2.1. Step 8 in Fig. 1 (a) checks whether the test set could meet the target fault coverage. Before compressing, redundant test patterns of valuable test patterns, which are stored in set U, must be eliminated by fault simulations. At step 9, we can obtain a test set U for deterministic testing.

Phase 2—Compression process. Since every deterministic test pattern only needs to store the corresponding LFSR vector and Johnson vector of p(t) and q(t) for set U, step 10 to step 11 can get the first time compressed test set V. Further analysis indicated that some test patterns in set V need to preserve only a same LFSR value and the number of test patterns because that these test patterns have the same LFSR. Since l-stage Johnson sequence has $2l$ different Johnson vectors and every vector consists of successive '0' or '1', a l-bit Johnson vector can be represented by a $(1+\lceil \log_2(2l) \rceil)$-bit binary digit, where $\lceil x \rceil$ is the least integer that is larger than or equal to x. The leftmost bit of this digit denotes the value of leftmost bit in the Johnson vector, and the remaining bits denote the number of consecutive bits that have the same value as that of the leftmost bit. In this way, we can get the second time compressed test set W, which is shown at step 12.

2.1 Extraction of the HC test sequence

Firstly, this section will introduce the generation method of the HC test sequence generated by step 1 to step 7 in Fig. 1 (a). This paper aims to search and generate the HC test sequence with following advantages: (a) Linear relations with consecutive vectors or within a vector. The benefit is to compress test data volume greatly. (b) The deterministic test set which is screened out from the HC test sequence by fault simulation should achieve the expected fault coverage. Based on the above, this paper converts Johnson sequences to low transition sequences for each scan chain. Vectors of two adjacent scan chains are within one clock delay, which enhances the compressible ratio of test data.

It is assumed that the sequential circuit with full-scan design has m primary inputs and M scan chains, and each scan chain contains l scan cells. At time t, the test vector is the bitwise exclusive OR result of the LFSR vector and Johnson vector, and vectors generated by the m-stage LFSR and the l-stage Johnson count are $S(t) = [S_0(t), S_1(t), \ldots, S_{m-1}(t)]$ and $J(t) = [J_0(t), J_1(t), \ldots, J_{l-1}(t)]$, respectively. The test vector applied to the i-th scan chain can be expressed as: $C_i(t,x) = \left[\sum_{j=1}^{l} S_i(t)x^{j-1} + J_i(t,x)\right] x^{(i-1)l}$, where $i \in (1, M)$ and $J_i(t,x)$ represents the corresponding polynomial of the i-th Johnson cyclic code. Thus, the test vector applied to the combinational logic of the CUT can be expressed as

$$X(t,x) = \sum_{j=1}^{m} S_{j-1}(t)x^{j-1} + \sum_{i=1}^{M}\left[\sum_{j=1}^{l} S_i(t)x^{j-1} + J_i(t,x)\right] x^{(i-1)l} \quad (1)$$

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Theorem 1: The maximal period of $X(t,x)$ is $2l(2^m-1)$

Proof: Because the period of Johnson sequence is $2l$, we have the following definitions at different time t and r: $p(t)=\lfloor t/(2l)\rfloor$, $q(t)=t-2lp(t)$, $p(r)=\lfloor r/(2l)\rfloor$, $q(r)=r-2lp(r)$, where $\lfloor x\rfloor$ is the greatest integer that is less than or equal to x. Thus,

$$X(t,x)+X(r,x)=\sum_{j=1}^{m}(S_{j-1}(t)+S_{j-1}(r))x^{j-1}+\sum_{i=1}^{M}\Big[J_{q(t)}(i,x)+J_{q(r)}(i,x)\Big]x^{(i-1)l}+\sum_{i=1}^{M}\left[\sum_{j=1}^{l}(S_{j-1}(p(t))+S_{j-1}(p(r)))x^{j-1}\right]x^{(i-1)l} \tag{2}$$

If $|p(t)-p(r)|\geq 1$, p(t) and p(r) are corresponding to different LFSR vectors. So:

$$\sum_{i=1}^{M}\left[\sum_{j=1}^{l}(S_{j-1}(p(t))+S_{j-1}(p(r)))x^{j-1}\right]x^{(i-1)l}\neq 0 \tag{3}$$

If $p(t)-p(r)=0$, Eq.2 can be simplified to

$$X(t,x)+X(r,x)=\sum_{j=1}^{m}(S_{j-1}(t)+S_{j-1}(r))x^{j-1}+\sum_{i=1}^{M}\Big[J_{q(t)}(i,x)+J_{q(r)}(i,x)\Big]x^{(i-1)l} \tag{4}$$

For a Johnson sequence, its vectors are unique. If Eq.4 is not equal to '0' for different q(t) and q(r), Eq.2 is also not equal to '0'. In addition, Eq.2 is not equal to '0' for a maximum length LFSR sequence by combining Eq.2 and Eq.3, and the periods of l-bit Johnson sequence and m-bit LFSR sequence are $2l$ and 2^m-1, respectively. Thus, the period of the sequence defined by Eq.1 is $2l(2^m-1)$. The theory presented above states that there are enough unique vectors. Also, there are linear relations between these vectors or within a vector.

Fig. 1 (b) shows symbolic representation for a generated pattern. In the first clock cycle, $J_0J_1J_2...J_{l-1}$ will be bit-XORed with $S_0S_1S_2...S_{m-1}$, and the results $X_1X_{l+1}X_{2l+1}...X_{(M-1)l+1}$ will be shifted into M scan chains, respectively. In the second clock cycle, $J_0J_1J_2...J_{l-1}$ will be circularly shifted as $J_{l-1}J_0J_1...J_{l-2}$ which will also be bit-XORed with seed $S_0S_1S_2...S_{m-1}$. Results $X_2X_{l+2}X_{2l+2}...X_{(M-1)l+2}$ will be shifted into M scan chains, respectively. After l clocks, M scan chains will be fully loaded with a unique test pattern, and seed $S_0S_1S_2...S_{m-1}$ will be applied to m primary inputs.

3 Compression algorithm and decompression mechanism

This section will firstly introduce the compression process. Symbolic simulations in Fig. 1 (b) state that an m-bit seed and an l-bit Johnson vector can be expanded to a HC pattern of $(m+l\times M)$ bits. Also, a LFSR seed keeps unchanged at most times. Therefore, the deterministic test patterns, which are screened out from the HC sequence by fault simulation at step 9 in Fig. 1 (a), can be compressed to their corresponding Johnson vectors and LFSR seeds. Assuming there are N test patterns in a test set which includes n($n\leq N$) different m-bit LFSR vectors. Supposing, too, the number of scan cells is N_{PPI}, the compression ratio (CR) can be expressed as:

$$CR=\frac{TS_U}{TS_C}=\frac{N(m+N_{PPI})}{n\times s+N(\lceil\log_2(2l)\rceil+1)} \tag{5}$$

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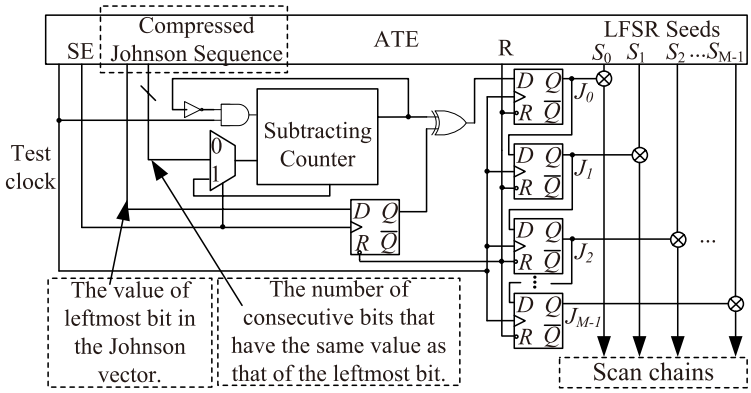

Fig. 2. Decompression architecture

where TS_U and TS_C represent the uncompressed deterministic test set and the compressed deterministic test set respectively, and s is the width of LFSR vector. For instance in s13207, there are 78832 HC test vectors for achieving high fault coverage. After fault simulations, we can obtain 428 deterministic test patterns which contribute to new fault coverage. Among the 428 test patterns, there are only 225 unique LFSR seeds. Since s13207 has 62 primary inputs (PIs) and 638 DFFs. So the storage of uncompressed test data can be calculated: $428 \times (62 + 638) = 299600$.

Since s13207 has 62 PIs, the stage of LFSR is 62. We determine the number of scan chains as 20, so the corresponding Johnson vector should be 32-bit width which can be represented by a 7-bit binary digit. The leftmost bit of this digit denotes the value of leftmost bit in the Johnson vector, and the remaining bits denote the number of consecutive bits that have the same value as that of the leftmost bit. For instance, 11111111110000000000000000000000 will be compressed to 1001010, of which the leftmost bit '1' denotes that the leftmost bit in the Johnson vector is '1', and '001010' represents the number of '1' in the Johnson vector is 10. We can also use 225 (2+62)-bit binary digits to represent 428 62-bit LFSR vectors. The leftmost two bits of every digit denote the number of patterns that have the same LFSR seed which is represented by the remaining 62 bits. So the compressed data storage is $225 \times (62 + 2) + 428 \times 7 = 17396$, and the compression ratio is $299600 \div 17396 \approx 17.2$.

The working mechanism of the decompressor is the reverse process of the compression algorithm. The main part of decompression circuit, shown in Fig. 2, is actually a linear decompressor which is composed of a subtracting counter and some assistant control circuits. The stored test data in ATE is the m-stage LFSR vectors and the compressed Johnson sequence. The linear decompressor decompresses a Johnson vector J_0, and J_0 will be circularly shifted as J_1. Similarly, J_1 will be circularly shifted as J_2 and so on. In this paper, $J_1, J_2, ..., J_{M-1}$ are called reconfigurable Johnson vectors. J_0 and reconfigurable Johnson vectors will bit-XOR with seed $S_0, S_1, ..., S_{M-1}$, and the results will be shifted into M scan chains, respectively. The overhead of decompression circuit will be discussed later.

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Table I. Performance of the proposed ATPG

Circuit	PIs+DFFs	SFC(%)		Prop.						CR		
				#Patterns	Stage(bit)		#Seed	DO	CR	[3]	[4]	[5]
		Prop.	[3]		Johnson	LFSR						
S13207	62+638	98.08	98.46	428	32	62	225	273	17.2	10.88	9.10	12.5
S15850	77+534	96.68	96.68	486	27	77	267	274	11.2	9.46	3.98	8.40
S38417	28+1636	97.50	99.47	986	82	28	259	289	111.8	25.86	2.81	3.85
S35932	35+1728	99.97	89.90	274	87	35	21	288	165.00	41.85	NA	NA
S38584	38+1426	99.39	95.85	727	72	38	434	290	47.40	22.86	3.45	4.26

4 Performance analysis of the proposed ATPGs

To analyze performances of the proposed ATPGs, experiments on full-scan designs of ISCAS'89 benchmarks are conducted. Synthesis and optimization are carried out using a SMIC 0.18 μm technology library. The test frequency is 100 MHz, and the power supply voltage is 1.1 V.

Table I compares the compression ratios of the proposed method with those in [3, 4, 5]. The column labeled 'SFC' shows the stuck-at fault coverage of the CUT. Sub-columns '#Patterns' and '#Seed' refer to the number of test patterns and the number of seeds, respectively. Compared with the method in [3, 4, 5], the proposed method demonstrates higher compression ratios.

The stuck-at fault coverage achieved by the proposed method with higher compression ratio is similar with that of [3]. In addition, the number of test patterns is relatively small because we adopt the deterministic testing method. It can be seen from Table I that the numbers of test patters are all less than 1000, which means the test time of the proposed is relatively short.

The overhead of the proposed decompressor is shown in the sub-column 'DO' of Table I in gate equivalents (a gate equivalent corresponds to a two-input NAND gate). The hardware overhead of [4] is approximately 377 to 582 gate equivalents. [5] only provided the overhead data of the decompressor used for s15850, and the number of gate equivalents is about 1900. It is obvious that the area occupied by the proposed decompressor is less than that of the above techniques with higher compression ratios.

5 Conclusion

This paper proposes a easily compressible ATPG method. It firstly develops a theory to express test sequence, and extracts a class of test sequences that has no repetitive vectors and has linear relationship between their vectors. On this basis, this paper develops an ATPG method, and analysis results show that the test patterns generated by this method show the favorable features of compressibility, uniqueness and low dependency relationship between fault coverage and TPG's initial states. Experiments on ISCAS'89 demonstrated that the proposed method can achieve a stuck-at fault coverage of more than 96%. Test compression ratios are over 10 for all benchmarks, and some ratios are over 100.

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