ELectronics EXpress

IEICE Electronics Express, Vol.8, No.24, 2025–2028

A novel large input range source-follower based filter architecture

Guy Torfs[1a)], **Zhisheng Li**[1], **Johan Bauwelinck**[1], **Jan Vandewege**[1], **and Peter Spiessens**[2]

[1] *Department of Information Technology, University Ghent*
Sint-Pietersnieuwstraat 41, 9000 Gent, Belgium

[2] *Essensium nv. Gaston Geenslaan 9, 3001 Leuven, Belgium*

a) *guy.torfs@intec.ugent.be*

Abstract: A novel large input range source-follower based filter architecture is proposed offering a increased 1-dB compression point, without increased power consumption. An alternative feedback mechanism enables single-ended use and simplifies the bias scheme. Simulation has confirmed a 250 MHz second order filter stage consuming 40 uA @ 1.2 V supply in a 0.13 um CMOS technology with 1-dB compression point at a differential peak to peak input amplitude of 1.4 V, more than doubling the input range of previous implementations with similar power dissipation.

Keywords: linearity, compression, source follower based filter, continuous-time filter

Classification: Integrated circuits

References

[1] X. Yin, J. Bauwelinck, G. Torfs, P. Demuytere, J. Vandewege, H. Tubbax, J. Wouters, P. Debacker, P. Spiessens, F. Stubbe, and J. Danneels, "Embedded ranging system in ISM band," *Electronics Letters*, vol. 44, no. 17, pp. 1043–1044, Aug. 2008.

[2] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter With 79-db DR," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2713–2719, Dec. 2006.

[3] H. Zhang, X. Li, S. Lai, and P. Ren, "A High-Linearity 264-MHz Source-Follower-Base Low-Pass Filter with High-Q Second-Order Cell for MB-OFDM UWB," *IEICE Trans. Electron.*, vol. E94-C, no. 6, pp. 999–1007, June 2011.

1 Introduction

The intelligence of portable wireless communication devices keeps increasing, while the limited battery capacity for this additional functionality doesn't. So, each sub-block needs to be optimized to get maximum performance out of as little power as possible. A critical building block in high bandwidth appli-

DOI: 10.1587/elex.8.2025
Received September 30, 2011
Accepted November 11, 2011
Published December 25, 2011

cations, such as UWB receivers and ranging receivers [1], is a continuous-time filter. Gm-C topologies are the common approach to realize low-power active filters at these high baseband frequencies and especially source-follower based filters [2] (Fig. 1) can be implemented with very low power consumption.

The circuit shown in Fig. 1 is very linear thanks to the inherent feedback present in a source-follower. The linearity will only be broken when the input signal increases the threshold voltage of the PMOS transistors. Linearity is especially important in a receiver front-end filter where high out of band interference can be expected, or where a higher gain is wanted to maximize the signal to noise ratio. [3] presents a solution that offers higher loop gain in the feedback path of the filter, this increases the linearity at the cost of additional power dissipation. This letter proposes a new source-follower based filter architecture that eliminates this linearity limitation without increasing the power consumption.

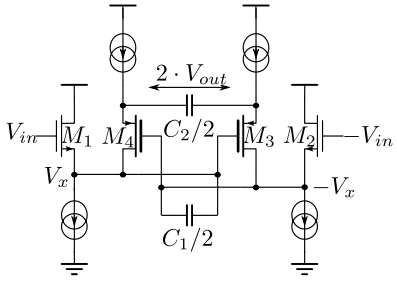

Fig. 1. Source-follower based filter proposed by [2]

2 Proposed Filter Architecture

The main linearity limitation in Fig. 1 occurs when large signals at nodes V_x or $-V_x$ becomes large enough to push transistors M_3 and M_4 in their linear region or even in their cut off region. We proposed the ciruit in Fig. 2 to overcome this problem.

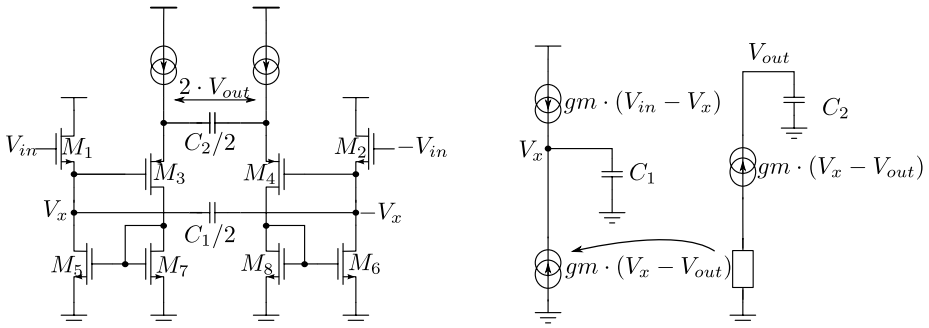

Fig. 2. (a) Proposed source-folower based filter and (b) its small signal equivalent

Instead of using transistors M_3 and M_4 to directly draw current out of C_1, the current is copied via current mirror M_5 and M_7 and current mirror M_6

DOI: 10.1587/elex.8.2025
Received September 30, 2011
Accepted November 11, 2011
Published December 25, 2011

and M_8 respectively. In this way the biasing scheme is simplified since the current for M_1 and M_2 is provided through the newly added current mirrors. Additionally, the cross-coupling used in Fig. 1 can be removed while keeping the current flowing through C_1 equal to $gm \cdot (V_{in} - V_{out})$, with gm equal to the transistors conductance. Hence, it becomes possible to use the filter in a single-ended configuration. The resulting transfer function is given by:

$$H(s) = -\frac{1}{s^2 \cdot \frac{C_1 C_2}{gm^2} + s \cdot \frac{C_1}{gm} + 1} \tag{1}$$

and the resulting filter parameters are:

$$\omega_0 = \frac{gm}{\sqrt{C_1 C_2}} \tag{2}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{3}$$

The small-signal linearity of the proposed filter architecture remains the same as the one of [2]. The non-linearity introduced by the current mirrors can be kept sufficiently small by increasing the length of the transistors and thus reducing the influence of channel length modulation to a minimum. A source-follower inherently shows high linearity because of the voltage feedback formed by $gm \cdot V_{GS}$, with V_{GS} equal to the transistors gate-source voltage. Again the effect of channel length modulation can be minimized by increasing the length of the transistors.

The main difference, though, occurs when considering large input signals. For in-band signals, M_1 and M_3 act as source followers. Transistor M_3 of Fig. 1 will enter the cut-off region due to the inverse relation of its drain and gate voltage, as depicted in Fig. 3 (a). Removing the cross-coupling and adding a low impedance connection to the drain of M_3, as proposed in Fig. 2, ensures sufficient head-room over the transistor (see Fig. 3 (b)). The solution proposed in this letter clearly eliminates the cut-off problem and guarantees linearity for larger input signals.

3 Results

The proposed filter has been validated by simulating and comparing its performance with [2] in a 0.13 um CMOS technology with a 1.2 V supply. Two 250 MHz filter stages, each consuming 40 uA, were designed according to the architectures of Fig. 1 and Fig. 2 respectively. To allow for a fair comparison between both designs, the transistors have been dimensioned and biased equally. A two tone input signal consisting of 50 MHz and 50.5 MHz has been applied and the deviation from the ideal linear and third order characteristic have been evaluated for different signal levels (see Fig. 3 (c-d)). The curve at Fig. 3 (c) reveals that the resulting 1-dB compression point is extended. Fig. 3 (d) shows that, in the proposed architecture, the point where strong non-linear effects occur and where the third order intermodulation starts deviating from its ideal charactertic is shifted to higher input powers. D'Amico's implementation [2] starts to show degradation when the output

DOI: 10.1587/elex.8.2025
Received September 30, 2011
Accepted November 11, 2011
Published December 25, 2011

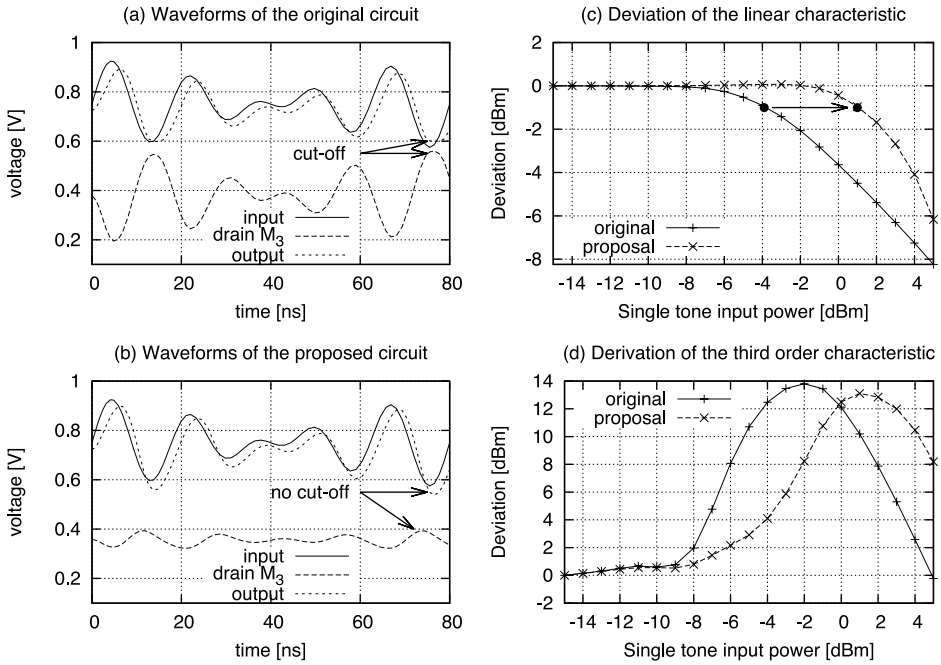

Fig. 3. (a) Waveforms of the original circuit (Fig. 1), (b) Waveforms of the proposed circuit (Fig. 2), (c) Deviation of the linear characteristic, (d) Deviation of the third order characteristic

transistors reach cut off. The proposed circuit degrades more slowly up to the point where the current sources driving M_3 and M_4 are forced in their linear region. As they provide the bias current for the output transistors as well as for the input transistors (through current mirrors M_5–M_7 and M_6–M_8, the current through the input transistors will be cut-off altogether. This happens when the (peak to peak) signal amplitude reaches 1.4 V, extending the linear input range with 5 dB (see Fig. 3 (c)).

4 Conclusion

A source-follower based filter with improved large signal linearity is presented. By removing the cross-coupling used in [2], while keeping the small signal behaviour identical, the output transistors are retained from entering their cut off region. This results in a linear input range covering very large input signals with amplitudes up to 1.4 Vpp differential at a 1.2 V supply. The current consumption remains unchanged compared to [2] and the biasing scheme is simplified in strong contrast with previously proposed techniques ([3]).

Acknowledgments

This work is supported by Essensium N.V. and by the Flemish Government under the IWT Grant 80334 ALOHA. The authors would like to thank the company for the fruitful discussions on the architectures.

DOI: 10.1587/elex.8.2025
Received September 30, 2011
Accepted November 11, 2011
Published December 25, 2011