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A novel architecture for low voltage-low power DLL-based frequency multipliers

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Abstract: New architecture for a DLL based frequency multiplier for wireless transceivers presents in this paper. This architecture has the advantages of occupying low area, low power, low voltage and low phase noise. Also good stability can be obtained in this design. This structure also can be used for generating big multiples of reference frequency. The proposed circuit can operate at a substantially low supply voltage**.** The circuit level and system level designs are presented. Also power consumption trade-offs are reported. Simulation results confirm the analytical predictions. The proposed DLL-based frequency multiplier is implemented in a 0.13um CMOS Technology.

Keywords: DLL, big multiplication, parallel architecture, frequency multiplier, Jitter

Classification: Integrated circuits

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1 Introduction

Delay locked loops find wide application in areas such as communication, clock skew, clock recovery circuits, digital circuits and frequency multiplier when accurate frequency is needed. DLLs are used because of their good jitters and phase noise performance and stability. Having fast locking time, easier to design and integrate loop filter are good features of DLLs rather than PLLs. The specific difference between DLLs and PLLs is that, DLLs use VCDL instead of VCO. So in DLLs jitters are only accumulated in one cycle which is not the same as PLLs, in which jitters are accumulated over multiple cycles. The main issue in a DLL-based frequency synthesizer is that the edge combiner just can synthesize small integer multiples of the reference frequency. In this work a new way is shown, which addresses this problem. Parallel of some DLLs are used to generate big multiples of the input frequency.

2 The proposed DLL-based frequency multiplier architecture

DLL-based frequency synthesizer is including a Voltage Controlled Delay Line (VCDL), a Phase-Frequency Detector (PFD), a Charge Pump (CP), First order Loop Filter (LF) and Edge Combiner. In a DLL, the input reference clock drives the delay line. The phase of the reference is compared to the phase of the delay line in the PFD. Depending on the time difference between the PFD input signals, a signal at the output of the PFD is generated. The CP provides a proportional charge which is integrated over the loop filter. Therefore, the loop filter's capacitor is charged or discharged if there is a time lead or time lag between the reference and the output of the delay line. The capacitor voltage (V_{cntl}) controls the delay of the delay elements of the delay line. Depending on the phase difference between the input reference clock and output of the last delay, it controls delay of any delay stage, till the two input signals become in-phase. When DLL is in lock, the edge combiner combines the edges of delay stages output's to get integer multiple of the input frequency.

When there is need to multiply the reference frequency with big multiplication factor (especially primary numbers), most of the time the conventional structure of DLL cannot be used. For example to generate 131 times of reference frequency with conventional structure of DLL-based frequency multipliers, 131 delay cells should be connected one after another (in series with each other) in VCDL. So it is obvious that 131 delay cells probably cannot satisfy the $N.\ t_{D,\min} \leq T_{ref}$ condition, where N is the number of delay cells in VCDL, $t_{D,min}$ is the minimum delay of each delay cells, and T_{ref} is the period of reference frequency. Even if this condition can be satisfied with special and optimized circuit design, we are faced with another problem, which is increasing in jitter contribution. The amount of jitter is directly proportional with number of delay cells in VCDL. So, it seems better to generate big multiplication factors with another structure.

Fig. 1.a shows the proposed structure for DLL-based frequency synthe-

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sizer. As it can be seen from this figure, to conquest this problem, parallel of some DLLs is used. Number of DLLs which are used in this architecture is related to maximum number of delay cells which can be used for each DLLs, maximum allowable jitter or phase noise in the design and the multiplication factor. It should be noted that unlike conventional DLLs structure, in this structure according to the design requirements, one or more delay cells in VCDL are different from the others. This new architecture can generate all big and small multiples of reference frequency by using multiple DLLs. To figure out the way that this structure works, an example will be introduced which is designed to generate 13 times of reference frequency. This process can be expanded to generate big multiples of reference frequency.

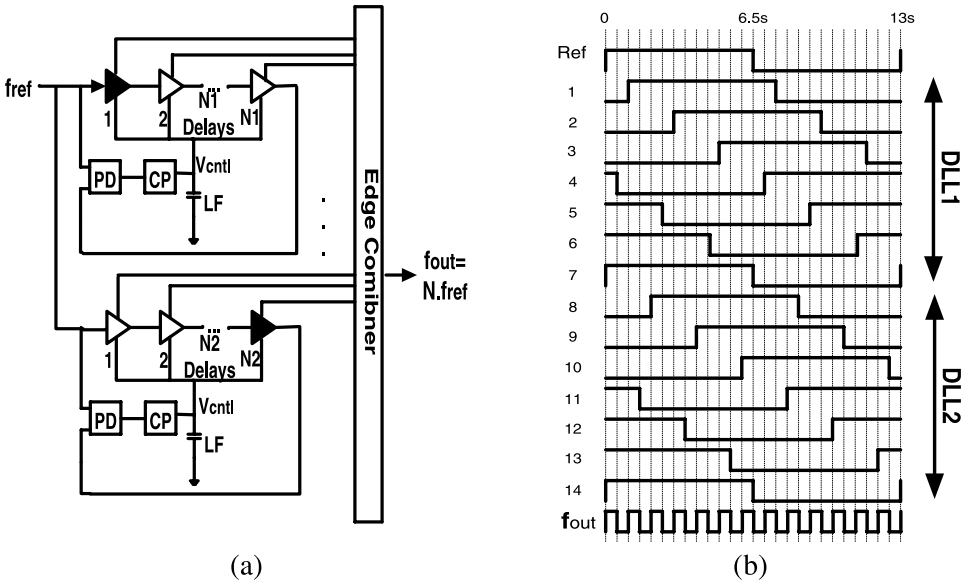

Fig. 1. (a) Proposed parallel structure for DLL-based frequency synthesizer (b) Waveforms of proposed structure with 14 delay cells and 2 DLLs

Suppose that T_{ref} =13 Sec and the goal is to generate 13 times of reference frequency with edge combiner (These assumptions are good choices for understanding of proposed structure). Edge combiner can generate 13 times of reference frequency (T_{ref}=13 Sec), if the VCDL has rising edges at $1, 2, \ldots, 13$ Sec. If the structure is designed in a way that these edges obtained, 13 times of reference frequency can be generated. To cover the goal of our example, we use structure of Fig. 1.a with 2 DLLs which are containing 7 delay cells in the VCDL. In the first DLL, the first delay cell should be designed in a way the that it's delay will be half of the others. Accordingly, the rising edges at 1, 3, 5, 7, 9, 11, 13 Sec can be generated with the first DLL. Also second DLL is containing of 7 delay cells in VCDL and the last delay cell's delay is half of the others. This DLL in its lock condition can generate rising edges at 2, 4, 6, 8, 10, 12, 13 Sec. With these edges and combining 13 from 14 outputs of VCDLs with XOR gates in edge combiner (one output is duplicated), 13 times of reference frequency can be generated. In

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Fig. 1.b waveforms of these two DLL in lock condition is shown. Waveforms 1 through 7 is related to first DLL and 8 through 14 is related to second DLLs. 7^{th} and 14^{th} outputs are the same and just one of them is used in edge combiner. It should be noted that delay of 1^{st} and 14^{th} delay cell is half of the others (1 Sec). In the rest of this paper for designing of DLL-based frequency multiplier f_{ref} is chosen 16 MHz and the goal is to generate the output frequency of 208 MHz (multiplication factor is 13). Hence with this structure all multiplication factors for example big multiplication factors or primary number factor can be generated.

3 Design of low power DLL-based frequency multiplier

The proposed DLL-based frequency synthesizer is implemented in a 0.13 um CMOS technology. All building blocks are implemented in a differential fashion to save the signals from the common mode noise. Only one common mode feedback circuitry is used to control the common mode voltage of the capacitors. The speed of common mode feedback is twice as much as that of the charge pump. Current Mode Logic (CML) family is used in the circuit design of the delay cells and the edge combiner. This section explains the circuit level realization of different blocks.

3.1 VCDL design

A CML buffer is used for each delay cells as reported in [1]. It consists of a pair of resistive loads, switches, and a constant tail current source. V_{cntl} controls the delays of delay stages. The propagation delay of each side is approximately:

$$t_D = RCLn2 \tag{1}$$

Where R is the resistance of PMOS loads. The proposed structure for generating 208 MHz frequency needs 14 delay cells, 7 for each DLL. From the above equations we get:

$$t_D = T/N_{\max} = 1/(6.5 \times 16 \times 10^6) = 9.61\,ns \tag{2}$$

We assume N=6.5 because each DLL contains one delay cell which has delay of half of the others. It should be noted that swing voltage of each delay cell is being fixed with using of replica delay cell method [2]. In this design V_{swing} is 0.3 V that means all of the inputs and outputs of delay stages are 1.2 V as high level voltage or 0.9 V as low level voltage. It should be noted that the delay cell which gives the delay of the half of the others, has the external capacitor about half of the others.

3.2 Phase-frequency detector design

A phase-frequency detector is designed based on the configuration reported in [3], which is shown in Fig. 2. The gates are implemented using differential CML gates. This implementation also rejects common-mode and power supply noise. Fig. 2.c shows the circuit topology of the NOR-gate. It should be noted that the levels of input for each Nor gates should be 0.9 V or 1.2 V. If

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somebody wants to use the lower level of voltage instead of 0.9 V, using of a level shifter and a buffer at the inputs of PFD are inevitable. In this design we use a level shifter and buffer for inputs of PFD to convert low level of voltage from 0.9 to 0.7 V, so PFD and CP are working with levels of 0.7 V and 1.2 V.

3.3 Charge pump and loop filter design

Fig. 2.d shows the circuit of the charge-pump (CP). It receives two differential inputs of UP and DOWN from the phase detector and provides a differential

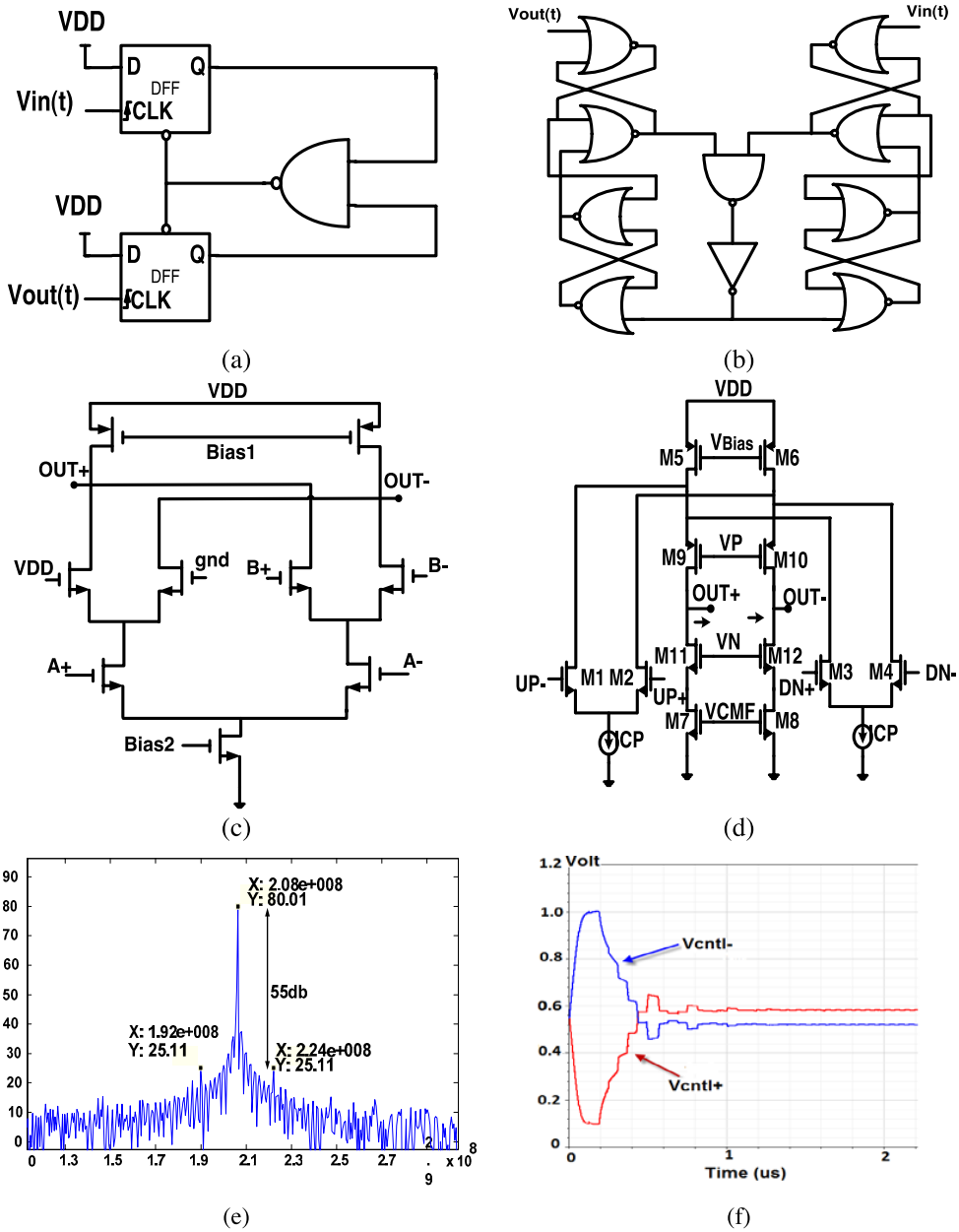

Fig. 2. (a) PFD Model, (b) Implementation of D-Flip Flop with Nor gates, (c) Circuit topology of Nor gate, (d) Circuit topology of Charge Pump (e) PSD of output, (f) Transition of V_{cntl+} *and* V_{cntl-} to achieve lock condition

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Table I. COMPARISON OF THIS WORK WITH OTHER

Author	Technology	Power Supply	Power	Lock Time	Phase Noise- Jitter
[4]	0.35um	3.3V	41.25 mW	50us	RMS(20ps@500MHz)
[5]	0.18um	1.8V	12 mW	10us	RMS(1.89ps@2GHz)
[6]	0.13um	1.2V	36 mW	----	RMS(1.06ps@5GHz)
[7]	0.09um	1V	45 mW	----	RMS(7.56ps@5GHz)
This Work	0.13um	1.2V	3.8 mW	2.5us	RMS(12ps@208MHz)

current to the output. In this topology, the current passing through M_6 and M_5 is set by a bias circuitry. The common mode feedback circuit sets the gate voltage of M_7 and M_8. If the circuit is in quiescent mode (i.e. both UP and DN signals are off), an equal amount of current is sunk from node A and B towards the input diff pairs. This makes an equal current to pass through M_9 and M_{10} which results in zero differential current at the output. If either UP or DN signal is activated the corresponding differential current of Icp is introduced at the output. The combination of PFD-CP provides charging current error of less than 2% over the entire range of output voltage swing under entire range of phase errors. It is shown later that $33\,\mu A$ is appropriate value for I_{CP}. The gain of PFD-CP is 0.01. So equation (3) can be obtained:

$$I_{cp} = 5.66 \times 10^6 C_{LF} \tag{3}$$

Hence with (3) and choosing of C_{LF}=5 pF, I_{CP} is calculated $28.3\,\mu A$. In this paper I_{CP} is chosen $33\,\mu A$ for better stability condition.

3.4 Edge combiner design

When DLL is in lock, the edge combiner combines the edges of delay stages output's to get integer multiple of the input frequency. For this design edge combiner consists of some XOR gates which are implemented in CML structure. These XOR gates have the same structure as NOR gates, which is shown in Fig. 2.c. It should be mentioned that these XOR gates is working with low level of 0.9 V and high level of 1.2 V.

4 Simulation results

When DLL is in lock condition, the PSD (power spectral density) of the proposed structure (Fig. 1) that generates f_{out}=208 MHz, using the reference frequency of f_{ref}=16 MHz and N=6.5 is shown in Fig. 2.e. Fig. 2.f is shown the locking process of the proposed DLL-based frequency synthesizer, which displays the variation of control voltages to reach the desirable value that is V_{cntl+} reaches to 0.6 V and V_{cntl-} reaches to 0.5 V at steady state. The phase noise is identical to the reference frequency's phase noise. The power dissipation in worst case is 3.8 mw and is really low for DLL-based frequency synthesizer design. A comparison of this work with other related works is shown in Table I. Low power, area, voltage, ability to generate big multiple of reference frequency and good jitter performance are the specific features of this design.

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5 Conclusion

In this paper, a DLL-based frequency multiplier in parallel form is presented. The propose structure imposes minimum phase noise and jitter due to its DLL nature. To minimize the phase offset good matching between UP/DOWN current in CP is established. Also the mismatch in delay cells and PFD elements are minimum. Also low power dissipation is announced. The architecture includes an edge combiner and with VCDL that have some different delay cells. It should be noticed that with this structure, big multiple of reference frequency can be obtained. The circuit level design with a fully differential realization of each blocks are presented. This novel architecture can be used for covering the frequency bands which need big multiplication factors.

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