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Scan power reduction based on clock-gating

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Abstract: The paper presents a new methodology to reduce scan test power by means of clock-gating. Scan-shift power is reduced through not clocking certain scan chains when they finish load/unload and scan-capture power reduction can be implemented by not clocking the scan chains in which there is no observation point. In addition, the corresponding hardware design is presented so as to show the feasibility of the new methodology. The algorithm for scan pattern reordering is also proposed to maximize the reduction of scan-shift power under certain constraint. Experimental results on several industrial designs have shown the effectiveness of this new methodology.

Keywords: scan-shift power, scan-capture power, load/unload cycles, observation requirement, clock-gating control

Classification: Integrated circuits

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1 Introduction

As we know, the full-scan design suffers from high test power dissipation. Excessive switching activity in scan chains and other parts of the circuit results in overheating and supply voltage noise. These may cause a device malfunction, yield loss, reliability degrading or even permanent damage of a circuit [1]. Existing methods such as partitioning [2, 3, 4], scan chain modification [5, 6], clock-gating [7, 8] can reduce power dissipation effectively during scan test. The X-filling methods [9, 10] are also commonly adopted since they can be used as a post-processing step in any ATPG flow. The method presented in [11] allows every scan chain to be driven by de-compressor or by constant value during entire scan load, so that the low power compression can be achieved. However, the method presented in [11] can't reduce the power consumption in the clock distribution network during scan shift. By controlling existing clock-gating, the method presented in [11] can reduce the peak power during scan capture. In this paper, we propose a novel methodology by utilizing clock-gating to reduce scan-shift power and scan-capture power simultaneously. For the scan chains which need less shift cycles, the clock-gating will block clocks when their load/unload procedures have finished. Since the scan-shift cycles are decided by the current pattern's load cycles and the last pattern's unload cycles, the patterns need to be specially reordered in order to maximize our methodology's benefit. Similarly, to reduce the scan-capture power, clock-gating can block clocks if the scan chains do not have observation points in certain pattern.

2 The methodology and corresponding hardware design

The hardware design based on clock-gating is shown in Fig. 1. The design is named scan-clock-control circuit and used to generate separate scan clock for each scan chain. The scan-clock-control circuit contains three parts: clock-gating cells $(CG_1, CG_2, \ldots, CG_n)$, shift registers $(S_1, S_2, \ldots, S_n)$ and update registers $(U_1, U_2, \ldots, U_n)$. Each clock-gating cell will generate a separate scan clock for one scan chain. The update registers are provided to hold the control-code while new data is shifted into shift registers through $ctrl\_code$ by using input clock $ctrl\_shift$.

The control-code mentioned in above paragraph is the key to our methodology and can be divided into two categories: shift-control-code and capture-control-code. The initial value of shift-control-code can be set in accordance with the following rules: for one bit, if there's no need to load or unload corresponding scan chain, set to 0, otherwise, set to 1. For certain pattern, the continuous clock has brought a waste of power consumption on the scan chains which need less shift cycles than others. When the load/unload procedures of those scan chains are finished, the clocks can be blocked by updating shift-control-code's corresponding bits from 1 to 0. The capture-control-code is used to block the clocks if there's no observation point in corresponding scan chains.

Based on the above analysis, the reduction on scan-shift power can be

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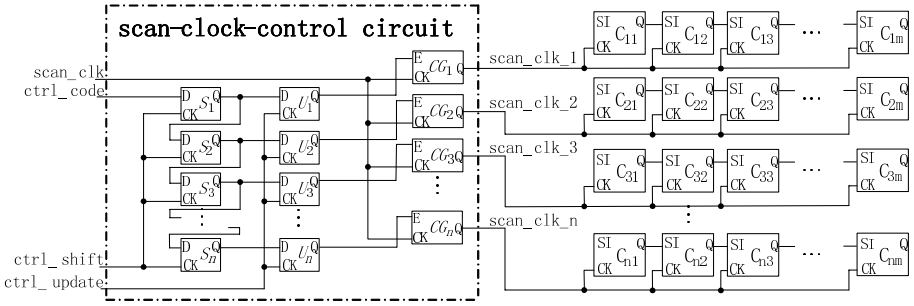

Fig. 1. scan-clock-control circuit

maximized if certain scan chains' clocks can be blocked as soon as corresponding load/unload procedures are finished. However, every update of shift-control-code requests the reloading on shift registers. If the time interval between two required updates is too short, it's impossible to implement such immediate update due to the hardware limitation. It's noteworthy that a time interval before scan capture procedure also needs to be preserved for loading capture-control-code. Normally the update number of shift-control-codes is decided by the scan structure. To avoid the overhead of test time, the quantity of shift-control-codes needs to be limited and thus each shift-control-code may include several updates. Obviously, the scan-shift power can be more reduced if more shift-control-codes can be adopted. In this paper, the number of shift-control-codes is set to 1 for further discussion.

Once the scan patterns have been generated and finally sorted, every pattern's requirement on shift cycles and observation can be easily got, and then the shift-control-code and capture-control-code can be calculated. Since the scan-clock-control circuit is independent, shifting and updating control-code can be implemented by applying simple test vectors via *ctrl_code*, *ctrl_shift* and *ctrl_update*. These additional test vectors will increase the test data volume a little but won't require any special ATPG algorithm. Moreover, they can be applied together with original scan patterns, so that our method won't bring any additional ATPG effort and test time. Since original scan patterns can be reused, the fault coverage won't be affected either. However, our method will slightly increase the area due to the added scan-clock-control circuit.

3 Algorithm for scan pattern reordering

To maximize the reduction of scan-shift power, we need reorder the scan patterns to pick up the optimum shift-control-code to be updated. Considering a design with m scan chains, we can define below parameters for each pattern.

$l_1, l_2, \ldots, l_m$: Required load cycles for each scan chain

$u_1, u_2, \ldots, u_m$: Required unload cycles for each scan chain

$f_1, f_2, \ldots, f_m$: Required load-unload cycles for each scan chain, f_i = Max $\{l_i$ of current pattern, u_i of next pattern$\}$

Besides the parameters for each pattern, we also define two sets as below.

O : Set containing the original patterns to be reordered.

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T : Set containing the reordered patterns.
To pick up the optimum shift-control-code and the right time to update, we need calculate the wasted power for every solution, then choose the best one. To simplify the calculation of wasted power, the sum of excess shift cycles can be used to evaluate all the solutions. The description of algorithm is as below:

```
for (every pattern in pattern list)
If (no pattern in T) {
for (every pattern in O)
Calculate the wasted power with l_i then record;
end for
Move the pattern with minimum wasted power to T;
} else {
for (every pattern in O)
Calculate f_i considering the last pattern in T;
for (every shift-control-code candidate)
Calculate the wasted power with f_i;
endfor
Pick the shift-control-code candidate with minimum wasted power;
end for
Move the pattern with minimum wasted power to T;
}
end for
```

With this algorithm, the optimum pattern order, shift-control-code and update time can be obtained simultaneously.

4 Experimental results

Experiments have been performed on several industrial designs and the results are shown in Table I. Compared with the method proposed in [11], the peak power of shift can be further reduced with our methodology. The method in [2] can get a better power reduction result than our method when there're 4 or more scan path partitions. Our peak capture power reduction percentage is low because we do not control existing clock-gating cells during pattern generation. It's noteworthy that our methodology doesn't conflict with scan segmentation in [2] and the clock-gating control method in [11].

Table I. Experimental results

Design	Gates	Scan Chains	Peak Shift Power Reduction (%)			Peak Capture Power Reduction (%)	
		(no × size)	Proposed	Method in [11]	Method in [2] (4 parts)	Proposed	Method in [11]
T161	360 K	107 × 199	61.73	56.28	75	5.61	25.32
T5572	1.6 M	297 × 239	69.26	63.15	75	6.93	26.81
T9283	2.9 M	288 × 297	73.58	67.98	75	4.52	30.05

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So the proposed methodology, together with the scan segmentation in [2] and the clock-gating control method in [11], can be used to further reduce scan test power.

5 Conclusion

We have presented a new methodology by utilizing clock-gating to reduce scan power. Unlike previous researches which use clock-gating only for capture power reduction, in our methodology both capture power and shift power are reduced by controlling clock-gating. Since original scan patterns can be reused, our methodology won't bring about any negative effect on ATPG effort, test time and fault coverage. However, our methodology will increase test data volume a little since additional simple test vectors are needed for shifting and updating control-code. Circuit area will also increase a little due to the added hardware. To maximize the benefit of this methodology, the algorithm for scan pattern reordering is also presented. The experimental results indicated the feasibility and the effectiveness of the proposed methodology.

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