

Design and implementation of equilateral triangle array digital direction finding system

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Abstract: In this work, a scheme of an equilateral triangle array digital direction finding system is proposed, which implements the online real-time direction finding task for an airborne system. The three-elements equilateral triangle array can be used for calibrating the channel errors and eliminating the DOA (direction of arrival) fuzzy problem of the two-elements linear array, which is greatly reduced the system complexity and suitable for portable requirement. At the same time, the project adopts field programmable gate array (FPGA) to process the sample data in parallel mode, including data quadrature demodulation and multiple signal classification (MUSIC) algorithm. The hardware implementation of MUSIC algorithm makes the system more flexible and faster than software implementation. The experimental results show that the deviation is less than 0.5 degrees with over 64 snapshots and the time is less 6 ms with 256 snapshots, and then the program can complete the MUSIC algorithm accurately with high speed.

Keywords: direction of arrival, equilateral triangle array, channel calibration, field programmable gate array, multiple signal classification algorithm

Classification: Electron devices, circuits, and systems

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1 Introduction

The high gate count and switching speed of modem FPGAs is enabling high data-rate DSP processing to be performed and achieve very complex high-speed Logic [1] without resorting to ASIC technology [2]. Static RAM based FPGAs also enable solutions to be re-programmable. Such soft solutions offer flexibility, which is an important attribute of a modem digital processing system.

Spatial spectrum estimation [3] is an important array signal technique which developed in the last 30 years, such as multiple signal classification algorithms (MUSIC) [4, 5], ESPRIT parameter estimation, weighted subspace fitting (WSF) and Higher-Order Cumulant method, etc. Theory and practice have proved that these algorithms have very high precision and high resolution. Although the spatial spectrum estimation theory has been in-





creasingly improved, but the main drawback of spatial spectral estimation algorithms for real-time location system is a large operation, with the difficulty of real-time implementation [6]. In paper [7], the author presents a practical implementation of FPGA based DOA estimator for wireless cellular base-station, but the signal source is not so far and the frequency is fixed, not suitable for our applications. For the requirements of real-time direction finding with high resolution for an airborne system, which at a time the outside signal number is 1 and the frequency is variable, we design an equilateral triangle array digital direction finding system. The scheme has a flexible and easy structure, whereas to solve the high complexity of MUSIC algorithm, we take full use of the advantage of the parallel processing capability of FPGA chips, and then give the MUSIC algorithm for hardware implementation. It also provides a self-calibration system [8] to achieve real-time calibration of the receiver channel by the equilateral triangle array combined with the DDS signal source, aiming to solve the problem of deterioration of the direction of arrival (DOA) estimation performance caused by channel amplitude and phase errors.

2 MUSIC algorithm for hardware implementation

The Conventional MUSIC algorithm requires a large number of complex operations. However, we can use a simple and effective pretreated algorithm [9] with real number operations instead of complex operations when the array is even-symmetric, greatly reducing the computational load and making the MUSIC algorithm faster.

Suppose the uniform linear array elements is N (N is even), and the response of the incident signal is X(t) = AS(t) + n(t), where X(t) for the array output; S(t) for the incident signal vector; n(t) for the noisy data vector; A for flow pattern matrix of space array, and then constructs a linear transformation matrix T as Eq. (1):

$$T = \begin{bmatrix} J & J \\ j\Gamma & -j\Gamma \end{bmatrix}_{N*N}$$
(1)

Where J is the unit matrix with dimension of N/2, Γ is the permutation matrix with dimension N/2 array (anti-diagonal elements are 1). The linear transformation defined as follows:

$$Y(t) = TX(t) = TAS(t) + Tn(t)$$
⁽²⁾

The real and imaginary parts of matrices Y(t) obtained from the transformation both contain phase information between array elements. So the real or imaginary part can be as the input for calculating covariance matrix. After the linear transformation, the MUSIC algorithm can be divided into three parts: covariance computation, singular value decomposition (SVD) and spectral peak search.

(a) Covariance computation, dealing with the N * M dimension real matrix (M for snapshots), multiplied with its transpose matrix and then get a





symmetric matrix with dimension N * N. This procedure is using N parallel multiply-adder structure to implementation and the parallel mode can greatly reduce the operation speed between N receiver channels.

(b) For SVD operation, the most popular for hardware implementation is Jacobi algorithm and QR algorithm [10, 11], but Jacobi algorithm is more accurate than the QR algorithm and easy for parallel implementation. So the Jacobi algorithm is more suitable for FPGA implementation.

(c) Peak search module is to calculate the number of signal sources and then calculate the pseudo-spectral function by using the information from SVD. In our application, due to that the signal number is 1, it does not need to estimate the signal number.

3 System hardware structure

The system adopted a superheterodyne receiver architecture, composed by the three channels, the detail realization of block diagram shown in Fig. 1:



Fig. 1. System block diagram.

3.1 Online calibrating system

The three antennas are Omni-directional antennas and the arrangement is an equilateral triangle. In the AFD (Analog front end), each antenna can be individually controlled by switching signals from FPGA module by the coupler. Each antenna can receipt signal from the outside or transmit the RF signal generated by the DDS source module. The implementation procedure of online calibration system is as follows: treated antenna 1 as transmitting antenna, antenna 2 and antenna 3 as receiving antennas, through the ADC and data analysis to estimate the amplitude and phase errors between channel 2 and channel 3, and then antenna 2 as transmitting antenna, antenna 1 and antenna 3 as receiving antennas, also through ADC and data analysis to





estimate the amplitude and phase errors between channel 1 and channel 3. After the above operations, we can get the whole amplitude and phase error information of 3 channels.

However, due to the characteristic of Omni-directional antenna, it will appear to be angle ambiguities of DOA based on two antennas. But if we adopt the equilateral triangle array mentioned above, the third antenna can be an assist to ensure the right DOA information of the target. After channel calibrating, we can implement the MUSIC algorithm based on 2-array elements searching from 0° to 360° between channel 2 and channel 3, channel 1 and channel 3. And finally by comparing the results of four angles, we can get the real target position.

3.2 DDS module

DDS signal source module generates the system clock for FPGA module and the external input clock for chip AD995x by using a 40 MHz OCXO, and then generates RF signal and LO signal. Due to the three channel design, the RF and LO signals are divided into three channels by the power dividers. And the system clock of FPGA module is also from the 40 MHz OXCO.

3.3 Data Acquisition & processing stage

The stage completes the function of system control, amplitude and phase error calculation and MUSIC algorithm. The system control will describe in Section. 4. Here we will focus on the data processing including baseband signal demodulation and hardware implementation of MUSIC algorithm.

For IF sampling mode, the baseband signal demodulation processing methods are mainly low-pass filtering, interpolation method and polyphase filter method [12, 13], and this paper adopts the low-pass filtering method based on FPGA, whereas the detail realization is given in reference [12] with the same author of this article.

The most difficult part for MUSIC algorithm is SVD calculation, but the high-order SVD calculation based on Jacobi algorithm can be divided into 2-order SVD calculation by parallel or recursive call architecture. So in the following, we will introduce the matrix with dimension 2*2 SVD calculation procedure, the equation is depicted as follows:

$$R(\theta_l)^T \begin{bmatrix} a & b \\ c & d \end{bmatrix} R(\theta_r) = \begin{bmatrix} \psi_1 & 0 \\ 0 & \psi_2 \end{bmatrix}$$
(3)

In Eq. (3), θ_l and θ_r are left-rotation angle and right-rotation angle, ψ_1 and ψ_2 are eigenvalues of SVD, and the rotation matrix is defined as:

$$R(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}$$
(4)

From Eq. (3) and Eq. (4), we can get an equation as:

$$\begin{cases} \theta_l + \theta_r = tan^{-1}(\frac{c+b}{d-a})\\ \theta_l - \theta_r = tan^{-1}(\frac{c-b}{d+a}) \end{cases}$$
(5)





For FPGA chip, operations including multiply, divide, sine, cosine, tangent, square root and exponential functions can be implemented by the CORDIC algorithm [14]. It needs only adder and shift operations, which can fully take the advantage of hardware to achieve fast calculation speed. The CORDIC state machine architecture is shown in Fig. 2:



Fig. 2. CORDIC state machine architecture.

4 System software design

The system adopted 89C52 microcontroller to control the whole system and communicate with the airborne system by RS422 interfaces. The main work flow is as follows:

(a) The power on self-test, waiting for the host serial port interrupt and receiving information;

(b) test the checksum of receiving information;

(c) obtain the working parameters, then select antenna 1 or antenna 2 as transmitting antenna and get the rest two channels sample data to analysis channel amplitude and phase errors;

(d) make the three antennas as receiving antennas to acquire the outside signals, and then compensate the channel and perform the MUSIC algorithm;

(e) send results to the host and wait for the next mission.

5 Test results

(a) In this closed-loop experiment, antenna 1 is as the transmitting antenna, while channel 2 and channel 3 as receiving channels. The standard RF signal source output power is 0 dBm, with 18° fixed angle. In different snapshots of 256, 128, 64, 32, 16, 8, 4, 2, and in different distance with the receiving power of -60 dBm, -71 dBm, the test results are shown in Table I:

From Table I: the angle error is less 0.5° when the RF power is -60 dBmand the snapshots in not less than 8; the angle error is less 0.5° when the RF power is -71 dBm and the snapshots in not less than 64. The more snapshots numbers, the more time needs for the MUSIC algorithm and less angle error.





| Power (dBm) | Snapshots /n | | | | | | | |
|-------------|--------------|-------|-------|-------|-------|-------|-------|-------|
| | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 |
| -60 | 17.93 | 17.93 | 17.93 | 17.93 | 18.28 | 18.28 | 17.58 | 15.82 |
| -71 | 17.93 | 17.93 | 17.58 | 17.23 | 18.98 | 19.34 | 15.12 | 25.31 |
| Time (ms) | 5.225 | 2.665 | 1.385 | 0.745 | 0.425 | 0.265 | 0.185 | 0.145 |

Table I. Test Results.

(b) The final compilation reports (by Quartus software ver7.1, FPGA: EP2C50F484C8) as follows:

total logical elements: 9 274 / 50 528 (18%); total memory bits: 409 600 / 594 432 (69%); Embedded Multiplier 9-bits elements: 102 / 172 (59%); total pins: 91 / 294 (31%).

6 Conclusion

This work presents an FPGA-based implementation of multi-channel digital direction finding system. The program takes full use of the capability of FPGA's parallel processing. Besides the real-time quadrature demodulation of multi-channel high-speed sample data, it also adopts a self-calibrating system to test the multi-channel amplitude and phase error in different frequency, allowing MUSIC algorithm based on FPGA for real-time performance stable and reliable, to achieve the engineering application.

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