ELectronics EXpress

IEICE Electronics Express, Vol.9, No.14, 1208–1213

Enhanced bootstrapped CMOS driver for large RC-load and ultra-low voltage VLSI

Hyeon-Jun Kim, Jong-Woo Kim, and Bai-Sun Kong[a)]

School of Information and Communication Engineering, Sungkyunkwan University

300 Chunchun-dong, Jangan-gu, Suwon, Gyunggi-do, 440–746, Korea

a) *bskong@skku.edu*

Abstract: This letter describes a novel bootstrapped CMOS driver for driving a large RC load in ultra-low voltage VLSI. The proposed driver eliminates the leakage from boosted nodes during bootstrapping operations, resulting in lower power consumption and higher switching speed. Since the proposed driver requires no additional transistors for eliminating the leakage, further improvements on switching speed and power consumption as well as layout area are achieved. Comparison results in a 0.13 μm CMOS technology indicated that the proposed bootstrapped CMOS driver achieved 82%∼18% improvements in terms of power consumption as compared to conventional bootstrapped CMOS drivers. They also indicated that the proposed driver achieved 42%∼11% improvements in terms of switching speed. Improvement on power-delay product (PDP) is as much as 160%∼30% as compared to conventional bootstrapped drivers.

Keywords: ultra low-voltage, bootstrapped driver, CMOS driver, sub-threshold driver

Classification: Integrated circuits

References

[1] A. Wang, A. Chandrakasan, and S. Kosonocky, "Optimal Supply and Threshold Scaling for Sub-threshold CMOS Circuits," *IEEE Computer Society Annual Symposium on VLSI*, pp. 5–9, April 2002.

[2] J. H. Lou and J. B. Kuo, "A 1.5 V full-swing bootstrapped CMOS large capacitive-load driver circuit suitable for low-voltage CMOS VLSI," *IEEE J.Solid-State Circuits*, vol. 32, no. 1, pp. 119–121, Jan. 1997.

[3] C. Y. Lu and C. T. Chuang, "Energy Efficient Bootstrapped CMOS Large RC-Load Driver Circuit for Ultra Low-Voltage VLSI," *Proc. IEEE International Symposium on VLSI Design, Automation, and Test (VLSI-DAT)*, Hsinchu, Taiwan, pp. 70–73, April 2010.

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012

IEICE Electronics Express, Vol.9, No.14, 1208–1213

1 Introduction

For reducing the power consumption of VLSI systems, the supply voltage can be scaled down that MOS transistors are made to be operated in the subthreshold region [1]. In emerging applications like wireless sensor networks and implantable medical devices, the supply voltage has been scaled down to the subthreshold region to increase the lifetime of a battery. But, a CMOS circuit operating in the subthreshold region is inappropriate for high-speed application because of severe speed degradation due to reduced gate-source voltage of MOS transistors. Long on-chip interconnect lines and some on-chip nodes having large RC loads further constrain the speed performance.

Using a bootstrapped CMOS circuit [2, 3] is a viable solution to overcome the drawback, which enhances the switching speed by forcing the gate voltage of transistors to be beyond the supply rails by capacitive coupling. But, the conventional bootstrapped CMOS driver in [2] inherently has a substantial amount of leakage, resulting in increased power and degraded speed. The conventional bootstrapped CMOS driver in [3] can eliminate the leakage, but since the driver uses a larger number of transistors, it still has large power consumption, degraded speed, and increased layout area.

This letter proposes a novel bootstrapped CMOS driver that addresses the leakage problem of the conventional bootstrapped driver in [2] in a more efficient manner than the approach presented in [3]. In Section 2, conventional bootstrapped drivers are described, and their limitations are discussed. In Section 3, the proposed bootstrapped driver is introduced and the operation principle is explained. Comparison results are discussed in Section 4, and conclusions are given in Section 5.

2 Conventional bootstrapped CMOS drivers

Conventional bootstrapped CMOS drivers are depicted in Fig. 1. Fig. 1 (a) shows one presented in [2], which consists of driver transistors (MP1 and MN1) for driving the output, and pull-up (MP2, MN3, MN4, and C_P) and pull-down (MN2, MP3, MP4, and C_N) bootstrap circuits for generating boosted voltages. When V_{IN} transitions from low to high, V_{INB} becomes low. Then, since MN4 and MP2 become off and MN3 becomes on, V_P and V_{PP} are boosted below the ground by capacitive coupling through C_P. Then, MP1 is turned on strongly to drive V_{OUT} high quickly. Similarly, when V_{IN} is falling, V_N and V_{NN} are boosted above VDD, allowing MN1 to be turned on strongly to drive V_{OUT} low quickly. However, the driver has a critical problem. Even though boosting capacitor C_P (C_N) provides enough charges to boost V_{PP} (V_{NN}) toward–VDD (2VDD), the established boosted voltage is far above (below) the required voltage due to leakages through transistors. For example, when V_{IN} is rising so that V_P and V_{PP} are to be boosted toward–VDD, MN4 turns slightly on since its source (V_P) has a lower voltage than its gate (V_{INB}), resulting in a gradual rise of the nodes due to the leakage through the transistor. Similarly, when V_{IN} is falling, V_N and V_{NN} wish to be boosted toward 2VDD, but are gradually discharged toward VDD

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012

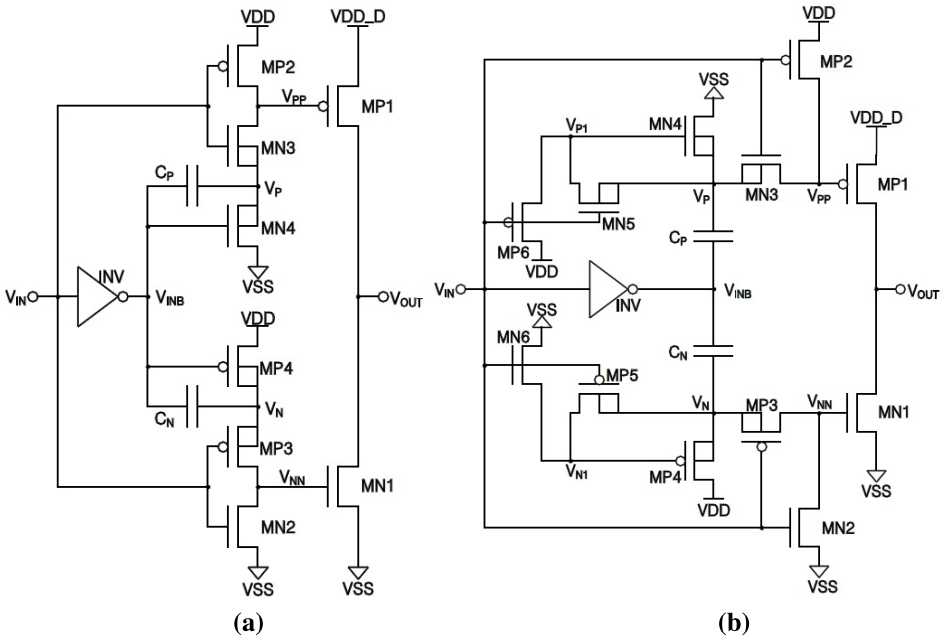


Fig. 1. Conventional bootstrapped CMOS drivers: (a) bootstrapped CMOS driver [2], (b) energy-efficient bootstrapped CMOS driver [3]

by the leakage through MP4. Shallow boosted voltages by these effects cause speed degradation.

Moreover, since the charges lost by the leakage in a cycle must be supplied in the next cycle, the overall power consumption is also increased.

To overcome the aforementioned problems, an energy-efficient bootstrapped CMOS driver shown in Fig. 1 (b) was proposed [3]. It uses four extra transistors (MN5, MN6, MP5, and MP6) to eliminate the leakage through MN4 and MP4 in the driver. During a negative bootstrapping, V_{P1}, the gate of MN4, is set to the negative boosted voltage (below ground) by MN5, letting the gate-source voltage of MN4 be zero. Then, the transistor becomes completely off, resulting in no leakage. Similarly, during a positive bootstrapping, V_{N1}, the gate of MP4, is set to the positive boosted voltage (above VDD) by MP5, letting the gate-source voltage of MP4 be zero to allow no leakage. Albeit no leakage, the driver still has some drawbacks. The dynamic power consumption becomes larger due to increased parasitic capacitance given by the extra transistors. The layout area also becomes larger due to increased device count. Moreover, the driver cannot provide with sufficiently high boosted voltages due to inherent charge loss from boosted nodes. That is, some of the charges boosted by a bootstrapping cannot be used for increasing the boosted voltage level, but must be transferred to charge the parasitic capacitance of V_{P1} or V_{N1}. So, the final boosted voltages become shallower than expected, resulting in speed degradation. In addition, the switching speed can be further degraded as the input capacitive load is increased.

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012

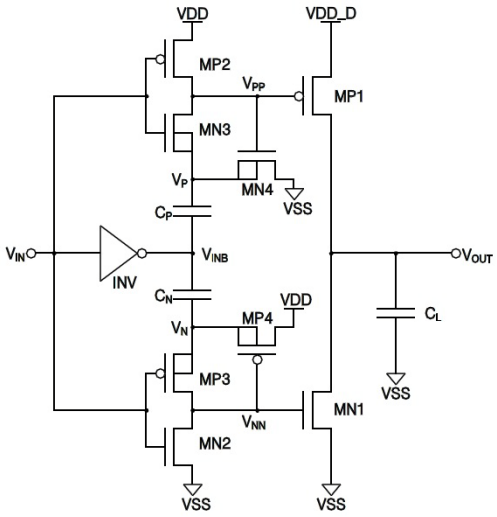


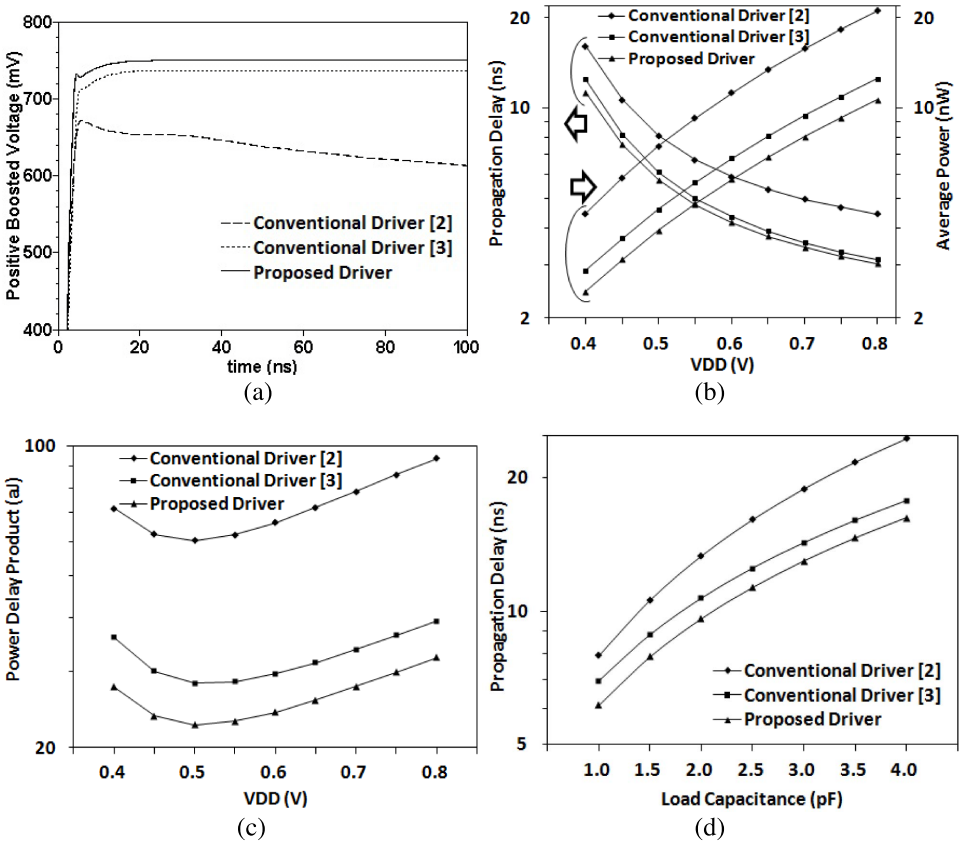
Fig. 2. Enhanced bootstrapped CMOS driver

3 Proposed bootstrapped CMOS driver

The proposed enhanced bootstrapped CMOS driver is shown in Fig. 2. It consists of driver transistors (MP1 and MN1) for driving the output and pull-up (MP2, MN3, MN4, and C_P) and pull-down (MN2, MP3, MP4, and C_N) bootstrap circuits for generating boosted voltages. The structure of the proposed driver is as simple as the conventional circuit in Fig. 1 (a), but the leakages through MN4 and MP4 are completely removed. When V_{IN} is low, V_{INB} is driven high by INV and node V_{PP} is high because MP2 is on and MN3 is off. As V_{PP} is high, node V_P becomes low by MN4. If V_{IN} is changed to high, MP2 and MN3 are turned off and on, respectively, and thus, V_{PP} is disconnected from the supply voltage and connected to V_P. At the same time, since V_{INB} transitions low by INV, both V_P and V_{PP} together are boosted below the ground by coupled capacitor C_P. Then, MN4 whose gate is connected to V_{PP} is turned off completely to cut off the leakage, and MP1 is turned on strongly to pull V_{OUT} up quickly. In a similar way, nodes V_N and V_{NN} are boosted above VDD by coupled capacitor C_N when V_{IN} is falling. MP4 then is turned off completely to eliminate the leakage, and MN1 is turned on strongly to pull down V_{OUT} rapidly.

As seen by the operation principle described above, the proposed driver has no leakage from boosted nodes. This feature allows more boosted charges to be used for voltage bootstrapping, leading to higher boosted voltage. As a result, the driving strength of driver transistors is more enhanced, leading to higher switching speed. No leakage from boosted nodes also allows less amount of charge drawn from the supply for the next bootstrapping, resulting in smaller power consumption. As compared to the conventional driver in Fig. 1 (b), the feature of using no additional transistors for eliminating the leakage leads to further power reduction since the total amount of parasitic capacitance in the circuit is reduced. The layout area will also be smaller. Moreover, since there is no need for boosted charges to be transferred to charge additional parasitic nodes, the final boosted voltages become higher,

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012



	Conventional (Fig. 1(a), [2])	Conventional Fig. 1(b), [3])	Proposed (Fig. 2)	Improvement (over [2]/[3], %)
Device Count (EA)	12	16	12	0 / 25
Input Capacitance (fF)	2.5	3.4	2.5	0 / 27
Positive ΔV_{BOOST} (mV)	270	337	350	23 / 4.0
Negative ΔV_{BOOST} (mV)	–270	–317	–325	17 / 2.5
t_P (for output rising, ns)	13.2	11.5	11.0	20 / 5.0
t_P (for output falling, ns)	16.1	12.5	11.3	42 / 11
Power consumption (nW)	4.45	2.88	2.44	82 / 18
Power-Delay Product (aJ)	71.7	35.9	27.6	160 / 30

(e)

Fig. 3. Comparison results: (a) boosted voltage waveforms (VDD = 400 mV), (b) delay and power versus VDD (C_L = 2.5 pF), (c) PDP versus VDD (C_L = 2.5 pF), (d) delay versus C_L (VDD = 400 mV), (e) performance summary (VDD = 400 mV, C_L = 2.5 pF)

resulting in higher switching speed. Lower input load also allows higher speed.

4 Comparison results

Bootstrapped CMOS drivers are designed in a 0.13 μm CMOS process. Bootstrap capacitors are implemented using MOS capacitance and equally set to be 30 fF, considering the trade-off between power-delay product and area overhead. To compare boosting efficiency, the voltages of V_{NN} of the drivers obtained at 0.4 V supply are compared in Fig. 3 (a). The boosted voltage

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012

of the driver in Fig. 1 (a) is the lowest and gradually falls down toward the supply voltage, since there is a substantial leakage through MN4. The driver in Fig. 1 (b) has higher boosted voltage and no fall-down of the boosted node by the elimination of the leakage. The proposed bootstrapped driver has the highest boosted voltage with no boosted voltage fall-down, indicating up to 23% improvement. The delay and power consumption of bootstrapped drivers operating at a supply voltage ranging from 0.4 V to 0.8 V are compared in Fig. 3 (b). The power consumption of the proposed driver is up to 82% lower than the conventional drivers. The propagation delay is also up to 42% smaller. The resulting power-delay product (PDP) shown in Fig. 3 (c) indicates that up to 160% improvement is obtained. Delay versus load capacitance is also shown in Fig. 3 (d), indicating that the performance gap becomes larger as load capacitance increases. The performance summary of bootstrapped drivers given in Fig. 3 (e) also indicates that the proposed driver has a superior performance. Specifically, as compared to recently published driver [3], the proposed driver has as much as 30% improvement in terms of PDP. The proposed driver also consumes 18% less power with up to 11% higher speed than. Device count and input capacitance are reduced by 25% and 27%, respectively.

5 Conclusion

A novel bootstrapped CMOS driver having no leakage from boosted nodes was proposed, resulting in high speed and low power. Use of no extra transistors for eliminating the leakage leads to further performance gain. Evaluation results indicated that the proposed driver would be well suited for driving a large RC load in ultra-low-voltage VLSI.

Acknowledgments

This work was sponsored by Industrial Strategic Technology Development Program funded by the Ministry of Knowledge Economy (MKE, Korea) (10039239, "Development of Power Management System SoC Supporting Multi-Battery Cells and Multi-Energy Sources for Smart Phones and Smart Devices"). This research was also supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0013702). Design tools were supported by IDEC, KAIST.

DOI: 10.1587/elex.9.1208
Received May 16, 2012
Accepted June 26, 2012
Published July 26, 2012